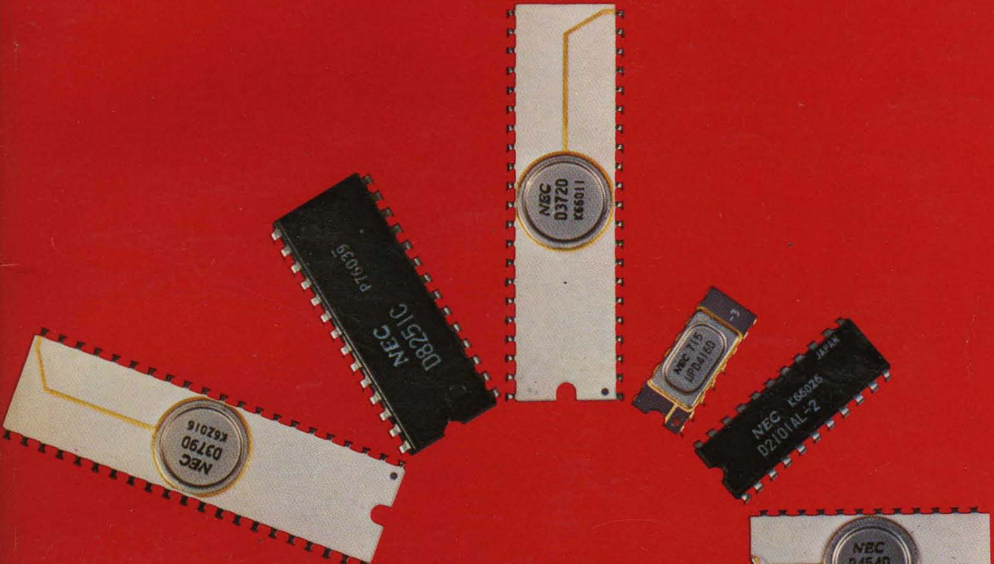
NEC Microcomputers, Inc.



Price $2.50

1979 Catalog

NEC

NEC Microcomputers, Inc.

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Mask Programmable ROMs

MEMORY SELECTION GUIDE

DEVICE	SIZE	TECHNOLOGY	ACCESS TIME	CYCLE	SUPPLY VOLTAGES	PACKAGE	
						MATERIAL	PINS
DYNAMIC RANDOM ACCESS MEMORIES							
μPD411	4K x 1 TS	NMOS	150 ns	380 ns	+12, +5, -5	D	22
μPD411-4	4K x 1 TS	NMOS	135 ns	320 ns	+15, +5, -5	D	22
μPD411A	4K x 1 TS	NMOS	200 ns	400 ns	+12, +5, -5	C	22
μPD416	16K x 1 TS	NMOS	120 ns	375 ns	+12, +5, -5	C/D	16
STATIC RANDOM ACCESS MEMORIES							
μPD443/6508	1K x 1 TS	CMOS	200 ns	200 ns	+5	C/D	16
μPD444/6514	1K x 4 TS	CMOS	300 ns	300 ns	+5	C	18
μPD445L	1K x 4 TS	CMOS	450 ns	450 ns	+5	C	20
μPD5101L	256 x 4 TS	CMOS	450 ns	450 ns	+5	C	22
μPD410	4K x 1 TS	NMOS	80 ns	220 ns	+12, +5, -5	C/D	22
μPD4104	4K x 1 TS	NMOS	85 ns	180 ns	+5	D	18
μPD2114L	1K x 4 TS	NMOS	200 ns	300 ns	+5	C	18
μPD2147	4K x 1 TS	NMOS	55 ns	55 ns	+5	D	18
μPD421 (F)	1K x 8 TS	NMOS	85 ns	85 ns	+5	D	22
MASK PROGRAMMED READ ONLY MEMORIES							
μPD2316E	2K x 8 TS	NMOS	450 ns	450 ns	+5	C/D	24
μPD2332	4K x 8 TS	NMOS	450 ns	450 ns	+5	C/D	24
μPD2364	8K x 8 TS	NMOS	450 ns	450 ns	+5	C/D	24
FIELD PROGRAMMABLE READ ONLY MEMORIES							
μPD2716 (F)	2K x 8 TS	NMOS	450 ns	450 ns	+5	D	24
μPD454	256 x 8 TS	NMOS	800 ns	800 ns	+12, +5*	D	24
μPD458	1K x 8 TS	NMOS	450 ns	450 ns	+12, +5*	D	28

Notes: (F) — Future Product
* — Read Mode
C — Plastic Package
D — Hermetic Package

MEMORY ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
AMD	AM2101	256 x 4 SRAM	μPD2101AL
	AM2101	1024 x 1 SRAM	μPD2102AL
	AM2111	256 x 4 SRAM	μPD2111AL
	AM9060	4096 x 1 DRAM	μPD411/μPD411A
	AM9101	256 x 4 SRAM	μPD2101AL
	AM9102	1024 x 1 SRAM	μPD2102AL
	AM9107	4096 x 1 DRAM	μPD411/μPD411A
	AM9111	256 x 4 SRAM	μPD2111AL
	AM9216	2048 x 8 ROM	μPD2316E
EM&M SEMI	4200	4096 x 1 SRAM	μPD410
	4300	4096 x 1 SRAM	μPD410
	4402	4096 x 1 SRAM	μPD410
	8108	1024 x 8 SRAM	μPD421
FAIRCHILD	2101L	256 x 4 SRAM	μPD2101AL
	2102	1024 x 1 SRAM	μPD2102AL
	3538	256 x 4 SRAM	μPD2101AL
	F16K	16384 x 1 DRAM	μPD416
FUJITSU	MB2114	1024 x 4 SRAM	μPD2114L
	MB8101	256 x 4 SRAM	μPD2101AL
	MB8107	4096 x 1 DRAM	μPD411/μPD411A
	MB8111	256 x 4 SRAM	μPD2111AL
	MB8116	16384 x 1 DRAM	μPD416
HARRIS	HM6501	256 x 4 SRAM	μPD5101L
	HM6508	1024 x 1 SRAM	μPD443/6508
	HM6514	1024 x 4 SRAM	μPD444/6514
INTERSIL	2616	2048 x 8 ROM	μPD2316E
	IM6508A	1024 x 1 SRAM	μPD443/6508
	7101	256 x 4 SRAM	μPD2101AL
	7111	256 x 4 SRAM	μPD2111AL
	7114	1024 x 4 SRAM	μPD2114L
	7116	16384 x 1 DRAM	μPD416
	7280/A	4096 x 1 DRAM	μPD411/μPD411A
	IM7552	512 x 1 SRAM	μPD2102AL
INTEL	2101	256 x 4 SRAM	μPD2101AL
	2102	1024 x 1 SRAM	μPD2102AL
	2107	4096 x 1 DRAM	μPD411/μPD411A
	2111	256 x 4 SRAM	μPD2111AL
	2114	1024 x 4 SRAM	μPD2114L
	2117	16384 x 1 DRAM	μPD416
	2147	4096 x 1 SRAM	μPD2147
	2316E	2048 x 8 ROM	μPD2316E
	2716	2048 x 8 EPROM	μPD2716
	5101	256 x 4 SRAM	μPD5101L
	8101A	256 x 4 SRAM	μPD2101AL
	8102A	1024 x 1 SRAM	μPD2102AL
	8111A	256 x 4 SRAM	μPD2111AL

MEMORY ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
MOSTEK	MK32000	4096 x 8 ROM	μPD2332
	MK34000	2048 x 8 ROM	μPD2316E
	MK36000	8192 x 8 ROM	μPD2364
	MK4102	1024 x 1 SRAM	μPD2102AL
	MK4104	4096 x 1 SRAM	μPD4104
	MK4116	16384 x 1 DRAM	μPD416
MOTOROLA	MCM2102	1024 x 1 SRAM	μPD2102AL
	MCM2111	256 x 4 SRAM	μPD2111AL
	MCM6616	16384 x 1 DRAM	μPD416
	MCM68111	256 x 4 SRAM	μPD2111AL
	MCM68317	2048 x 8 ROM	μPD2316E
NATIONAL	MM2101	256 x 4 SRAM	μPD2101AL
	MM2102A	1024 x 1 SRAM	μPD2102AL
	MM2111	256 x 4 SRAM	μPD2111AL
	MM5280A	4096 x 1 DRAM	μPD411/μPD411A
	MM5281	4096 x 1 DRAM	μPD411/μPD411A
	MM74C920	256 x 4 SRAM	μPD5101L
SIGNETICS	2101	256 x 4 SRAM	μPD2101AL
	2102	1024 x 1 SRAM	μPD2102AL
	2111	256 x 4 SRAM	μPD2111AL
	2316	2048 x 8 ROM	μPD2316E
	2601	256 x 4 SRAM	μPD2101AL
	2611	256 x 4 SRAM	μPD2111AL
	2680	4096 x 1 DRAM	μPD411/μPD411A
T.I.	TMS2101	256 x 4 SRAM	μPD2101AL
	TMS2102	1024 x 1 SRAM	μPD2102AL
	TMS4033	1024 x 1 SRAM	μPD2102AL
	TMS4034	1024 x 1 SRAM	μPD2102AL
	TMS4039	256 x 4 SRAM	μPD2101AL
	TMS4042	256 x 4 SRAM	μPD2111AL
	TMS4044	1024 x 4 SRAM	μPD2114L
	TMS4060	4096 x 1 DRAM	μPD411/μPD411A
	TMS4116	16384 x 1 DRAM	μPD416
	TMS4732	4096 x 8 ROM	μPD2332

NEC Microcomputers, Inc.

NEC

µPD411-E
µPD411
µPD411-1
µPD411-2
µPD411-3
µPD411-4

FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION

The µPD411 Family consists of six 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The µPD411 Family is designed using dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is a non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

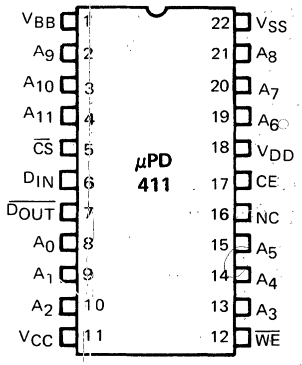
All of these products are guaranteed for operation over the 0 to 70°C temperature range.

Important features of the µPD411 family are:

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power/0.3 mW (Typ.)
- Power Supply: +12, +5, −5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Ceramic Dual-in-Line Package
- Replacement for INTEL'S 2107B, TI'S 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
µPD411-E	350 ns	800 ns	960 ns	1 ms
µPD411	300 ns	470 ns	650 ns	2 ms
µPD411-1	250 ns	470 ns	640 ns	2 ms
µPD411-2	200 ns	400 ns	520 ns	2 ms
µPD411-3	150 ns	380 ns	470 ns	2 ms
µPD411-4	135 ns	320 ns	320 ns	2 ms

PIN CONFIGURATION



Rev/2

PIN NAMES

A_0 - A_{11}	Address Inputs
A_0 - A_5	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	Power
NC	No Connection

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

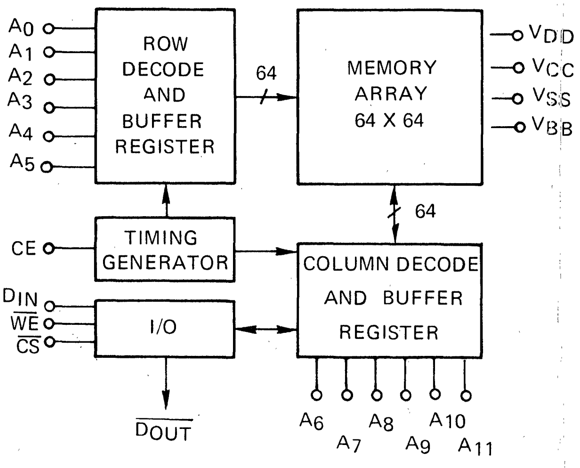
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*µPD411-E = 1 millisecond refresh period.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

	µPD411 FAMILY (EXCEPT 411-4)	µPD411-4
Operating Temperature	0°C to +70°C	+10°C to +55°C
Storage Temperature	−55°C to +150°C	−55°C to +150°C
All Output Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
All Input Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{DD}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{CC}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Power Dissipation	1.0W	1.5W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = 5V ±5%, V_{SS} = 0V,
Except V_{DD} = +15V ±5% for 411-4.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ①	MAX		
Input Load Current	I_{LI}		0.01	10	µA	V_{IN} = $V_{IL\,MIN}$ to $V_{IH\,MAX}$
CE Input Load Current	I_{LC}		0.01	10	µA	V_{IN} = $V_{ILC\,MIN}$ to $V_{IHC\,MAX}$
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_0 = 0V to 5.25V
V_{DD} Supply Current during CE off	$I_{DD\,OFF}$		20	200	µA	CE = 1.0V to 0.6V
V_{DD} Supply Current during CE on	$I_{DD\,ON}$		35[6]	60[5]	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
µPD411-E	$I_{DD\,AV}$		29	60	mA	Cycle Time = 800 ns
µPD411	$I_{DD\,AV}$		37	60	mA	Cycle Time = 470 ns
µPD411-1	$I_{DD\,AV}$		37	60	mA	Cycle Time = 470 ns
µPD411-2	$I_{DD\,AV}$		37	60	mA	Cycle Time = 400 ns
µPD411-3	$I_{DD\,AV}$		41	65	mA	Cycle Time = 380 ns
µPD411-4	$I_{DD\,AV}$		55	80	mA	Cycle Time = 320 ns
V_{BB} Supply Current ②	I_{BB}		5	100	µA	
V_{CC} Supply Current during CE off ③	$I_{CC\,OFF}$		0.01	10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	-1.0		0.6	V	
Input High Voltage	V_{IH}	2.4 ④		V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	-1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}-1	V_{DD}	V_{DD}+1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -2.0 mA

Notes:
① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
④ 3.5V for µPD411-E
⑤ 65 mA for µPD411-3
80 mA for µPD411-4
⑥ 41 mA for µPD411-3
55 mA for µPD411-4

CAPACITANCE

T_a = 0° – 70°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Capacitance, $\overline{CS}$	C_{AD}		4	6	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pF	V_{IN} = V_{SS}
Data Output Capacitance	C_{OUT}		5	7	pF	V_{OUT} = 0V
D_{IN} and $\overline{WE}$ Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
Cycle Time	t_{CY}	800		470		470		400		380		320		ns
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	210	3000	200	3000	ns
CE Output Delay	t_{CO}		330		280		230		180		130		115	ns
Access Time	t_{ACC}		350		300		250		200		150		135	ns
CE to $\overline{WE}$	t_{WL}	40		40		40		40		40		40		ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		0		ns

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CY}	800		470		470		400		380		320		ns
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	210	3000	200	3000	ns
$\overline{WE}$ to CE off	t_W	200		180		180		150		150		65		ns
CE to $\overline{WE}$	t_{CW}	380		300		260		230		210		200		ns
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		40		ns
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		100		65		ns

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

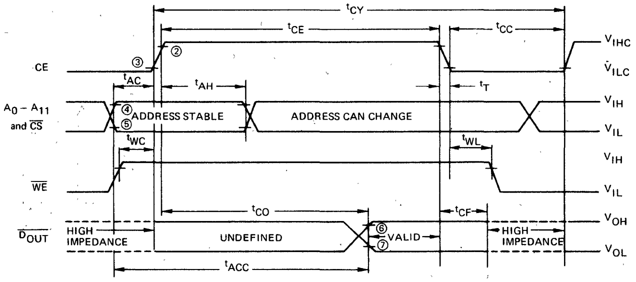
READ-MODIFY-WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read—Modify—Write (RMW) Cycle Time	t_{RWC}	960		650		640		520		470		320		ns
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	300	3000	200	3000	ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		0		ns
$\overline{WE}$ to CE off	t_W	200		180		180		150		150		65		ns
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		100		65		ns
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		40		ns
CE to Output Display	t_{CO}		330		280		230		180		130		115	ns
Access Time	t_{ACC}		350		300		250		200		150		135	ns

TIMING WAVEFORMS

READ CYCLE ①



Notes: ① For refresh cycle row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} −2V is the reference level for measuring timing of CE.

③ V_{SS} +2V is the reference level for measuring timing of CE.

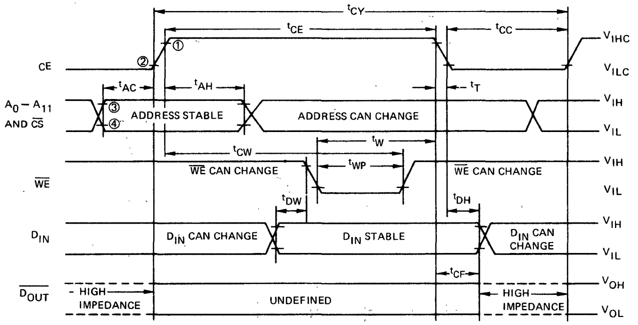
④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑥ V_{SS} +2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} +0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

WRITE CYCLE



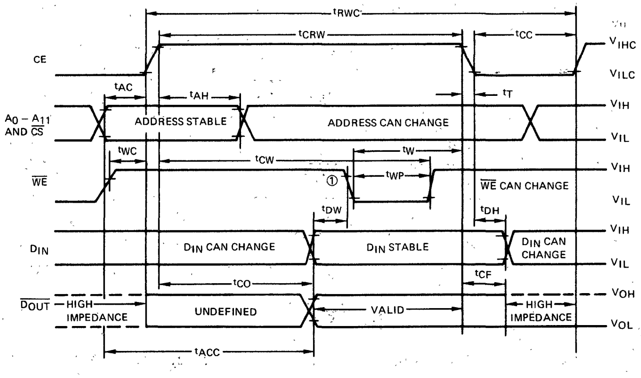
Notes ① V_{DD} −2V is the reference level for measuring timing of CE

② V_{SS} +2V is the reference level for measuring timing of CE.

③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

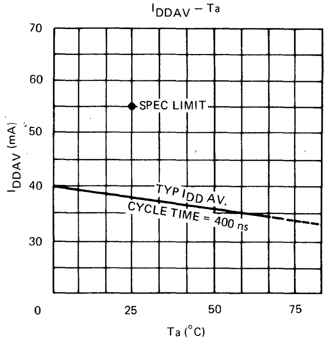
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

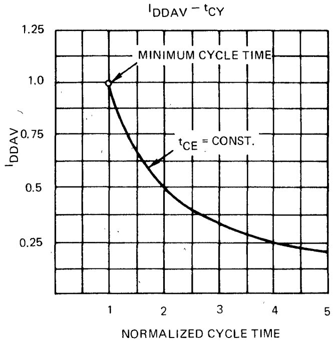
READ-MODIFY-WRITE CYCLE

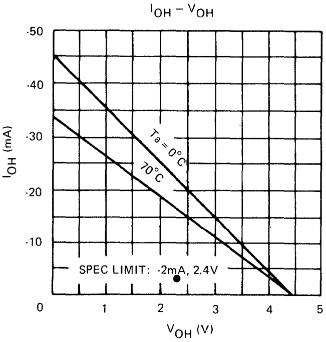


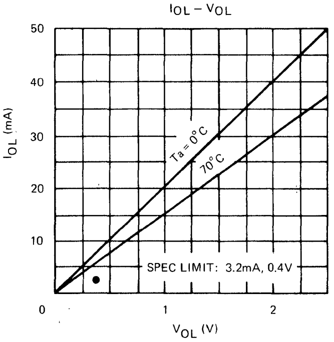
Note: ① $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

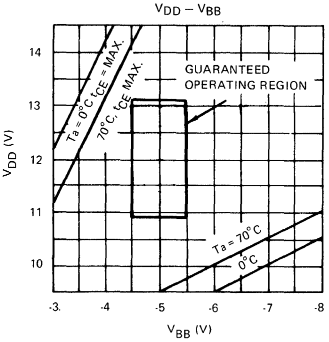
TYPICAL OPERATING CHARACTERISTICS (Except 411-4)

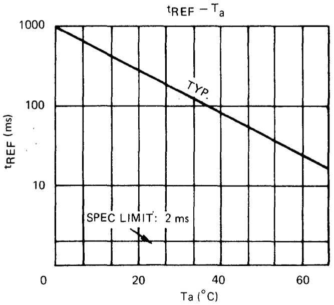












POWER CONSUMPTION

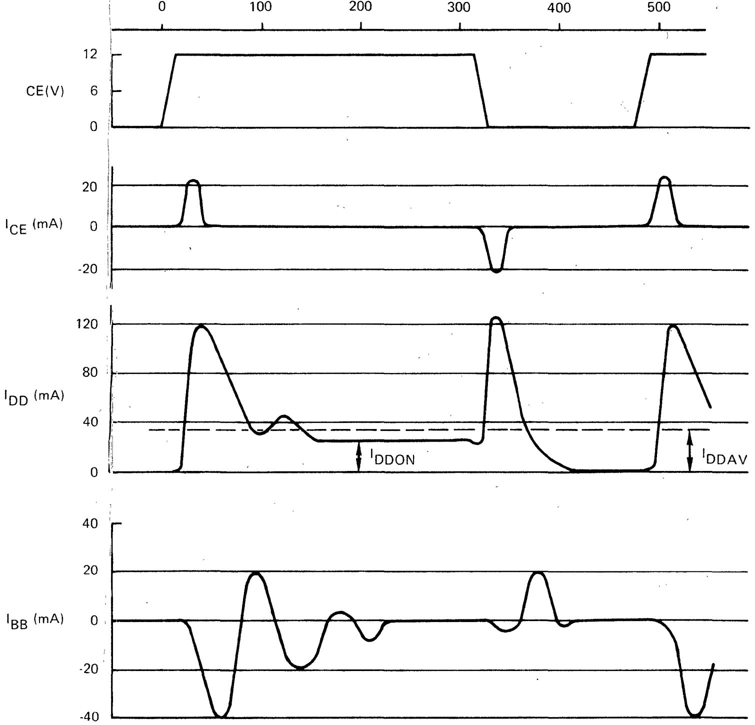
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$.

Typical power dissiption for each product is shown below.

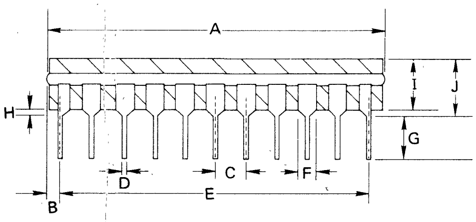
	mW (TYP.)	CONDITIONS
μPD411-E	350	Ta = 25° C, t_{cy} = 800ns, t_{CE} = 380ns
μPD411	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 300ns
μPD411-1	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 260ns
μPD411-2	450	Ta = 25° C, t_{cy} = 400ns, t_{CE} = 230ns
μPD411-3	550	Ta = 25° C, t_{cy} = 380ns, t_{CE} = 210ns
μPD411-4	660	Ta = 25° C, t_{cy} = 320ns, t_{CE} = 200ns

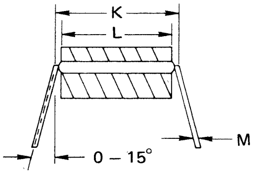
See above curves for power dissipation versus cycle time.

CURRENT WAVEFORMS



PACKAGE OUTLINE
μPD411D





ITEM	MILLIMETERS	INCHES
A	27.43 MAX	1.079 MAX
B	1.27 MAX	0.05 MAX
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 MAX	0.165 MAX
J	5.08 MAX	0.200 MAX
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

NEC Microcomputers, Inc.

μPD411A-E
μPD411A
μPD411A-1
μPD411A-2

4096 BIT DYNAMIC RAMS

DESCRIPTION

The μPD411A Family consists of four 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411A Family is designed using dynamic circuitry which reduces the standby power dissipation.

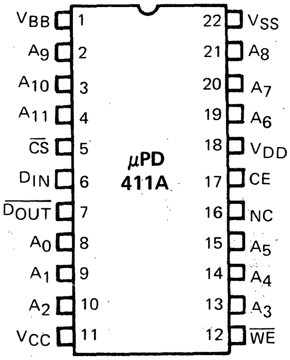
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power 0.7 mW (Typ.)
- Power Supply +12, +5, –5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Plastic or Cerdip Dual-in-Line Package
- Replacement for INTEL's 2107B, TI's 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411A-E	350 ns	800 ns	960 ns	1 ms
μPD411A	300 ns	470 ns	650 ns	2 ms
μPD411A-1	250 ns	430 ns	600 ns	2 ms
μPD411A-2	200 ns	400 ns	520 ns	2 ms

PIN CONFIGURATION



PIN NAMES

A_0 - A_{11}	Address Inputs
A_0 - A_5	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	(Powe. –5V)
NC	No Connection

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

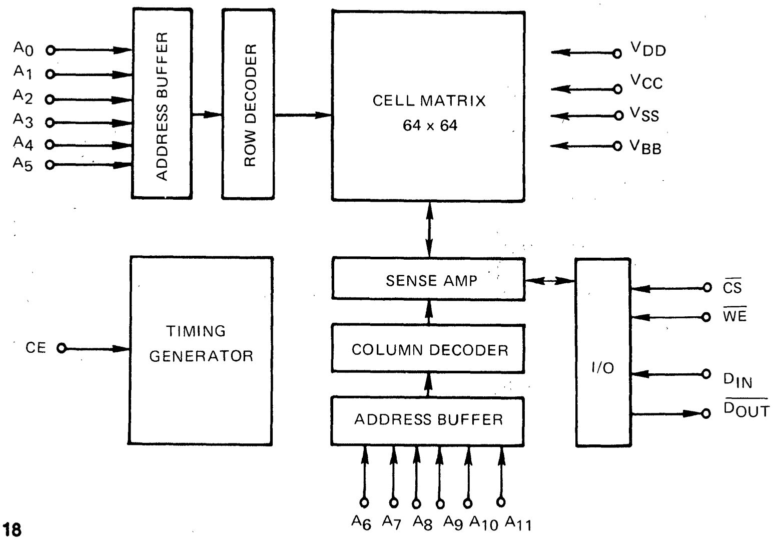
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411A-E = 1 millisecond refresh period.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Output Voltage ①	+20 to −0.3 Volts
All Input Voltages ①	+20 to −0.3 Volts
Supply Voltage V_{DD} ①	+20 to −0.3 Volts
Supply Voltage V_{CC} ①	+20 to −0.3 Volts
Supply Voltage V_{SS} ①	+20 to −0.3 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	TYP. ①	MAX.	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	µA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
CE Input Load Current	I_{LC}		0.01	10	µA	$V_{IN} = V_{ILC\,MIN}$ to $V_{IHC\,MAX}$
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	$I_{DD\,OFF}$		50	200	µA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	$I_{DD\,ON}$		35	50	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
µPD411A-E	$I_{DD\,AV}$		25	40	mA	Cycle Time = 800 ns
µPD411A	$I_{DD\,AV}$		38	55	mA	Cycle Time = 470 ns
µPD411A-1	$I_{DD\,AV}$		38	55	mA	Cycle Time = 430 ns
µPD411A-2	$I_{DD\,AV}$		38	55	mA	Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	µA	
V_{CC} Supply Current during CE off ③	$I_{CC\,OFF}$		0.01	10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} − 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			6	pF	$V_{IN} = V_{SS}$
$\overline{CS}$ Capacitance	C_{CS}			6	pF	$V_{IN} = V_{SS}$
D_{IN} Capacitance	C_{IN}			6	pF	$V_{IN} = V_{SS}$
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	$V_{OUT} = V_{SS}$
$\overline{WE}$ Capacitance	C_{WE}			7	pF	$V_{IN} = V_{SS}$
CE Capacitance	C_{CE1}			27	pF	$V_{IN} = V_{SS}$
	C_{CE2}			22	pF	$V_{IN} = V_{DD}$

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

		LIMITS									
		μPD411A-E		μPD411A		μPD411A-1		μPD411A-2			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	TEST CONDITIONS
Time Between Refresh	t_{REF}		1		2		2		2	ms	t_T = t_r = t_f = 20 ns C_L = 50 pF Load = 1$_{TTL}$ Gate V_{ref} = 2.0 or 0.8 Volts
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
Cycle Time	t_{CY}	800		470		430		400		ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
CE Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	
CE to $\overline{\text{WE}}$	t_{WL}	40		40		40		40		ns	
$\overline{\text{WE}}$ to CE on	t_{WC}	0		0		0		0		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

		LIMITS									
		μPD411A-E		μPD411A		μPD411A-1		μPD411A-2			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CY}	800		470		430		400		ns	t_T = t_r = t_f = 20 ns C_L = 50 pF Load = 1$_{TTL}$ Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
$\overline{\text{WE}}$ to CE off	t_W	200		180		180		150		ns	
CE to $\overline{\text{WE}}$	t_{CW}	380		300		260		230		ns	
D_{IN} to $\overline{\text{WE}}$ Set Up ①	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
$\overline{\text{WE}}$ Pulse Width	t_{WP}	200		180		180		150		ns	

Note: ① If $\overline{\text{WE}}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

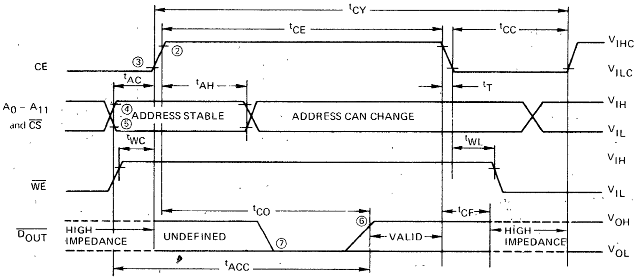
READ-MODIFY-WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

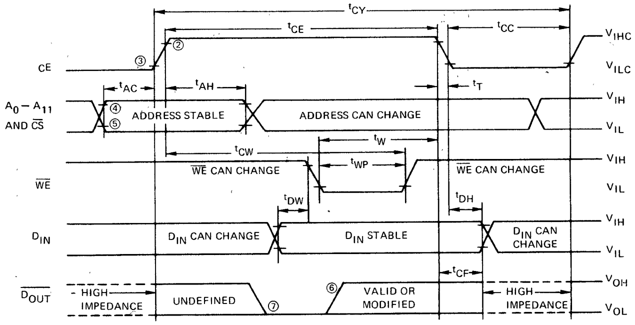
		LIMITS									
		μPD411A-E		μPD411A		μPD411A-1		μPD411A-2			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	TEST CONDITIONS
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	960		650		600		520		ns	t_T = t_r = t_f = 20 ns C_L = 50 pF Load = 1$_{TTL}$ Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	ns	
$\overline{\text{WE}}$ to CE on	t_{WC}	0		0		0		0		ns	
$\overline{\text{WE}}$ to CE off	t_W	200		180		180		150		ns	
$\overline{\text{WE}}$ Pulse Width	t_{WP}	200		180		180		150		ns	
D_{IN} to $\overline{\text{WE}}$ Set Up	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
CE to Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	

TIMING WAVEFORMS

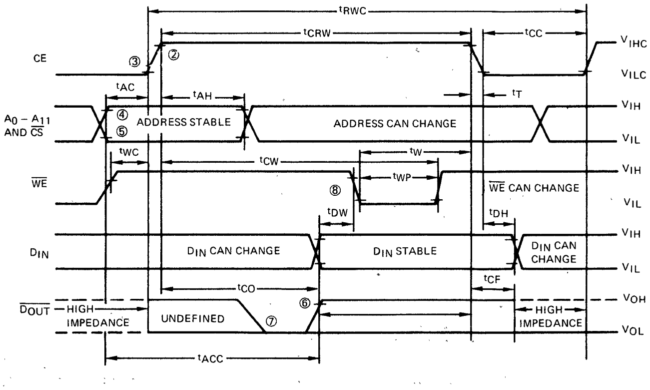
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② $V_{DD} - 2V$ is the reference level for measuring timing of CE.

③ $V_{SS} + 2V$ is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

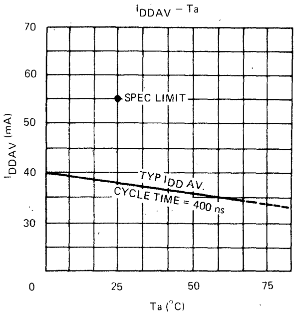
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

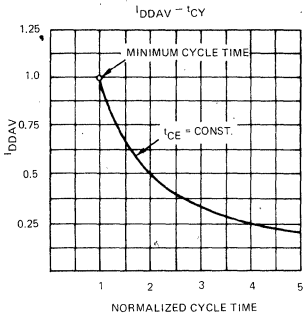
⑥ $V_{SS} + 2.0V$ is the reference level for measuring timing of $\overline{D_{OUT}}$.

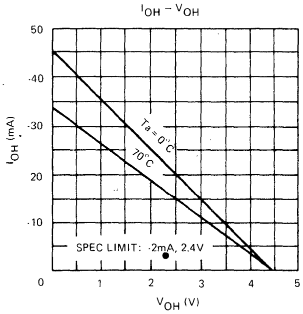
⑦ $V_{SS} + 0.8V$ is the reference level for measuring timing of $\overline{D_{OUT}}$.

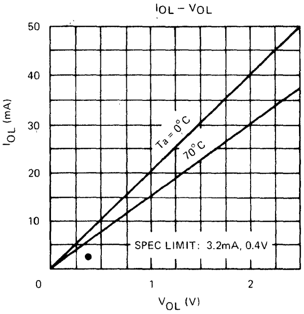
⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

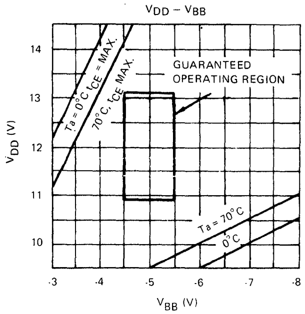
TYPICAL OPERATING CHARACTERISTICS

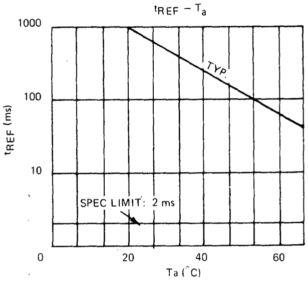












POWER CONSUMPTION

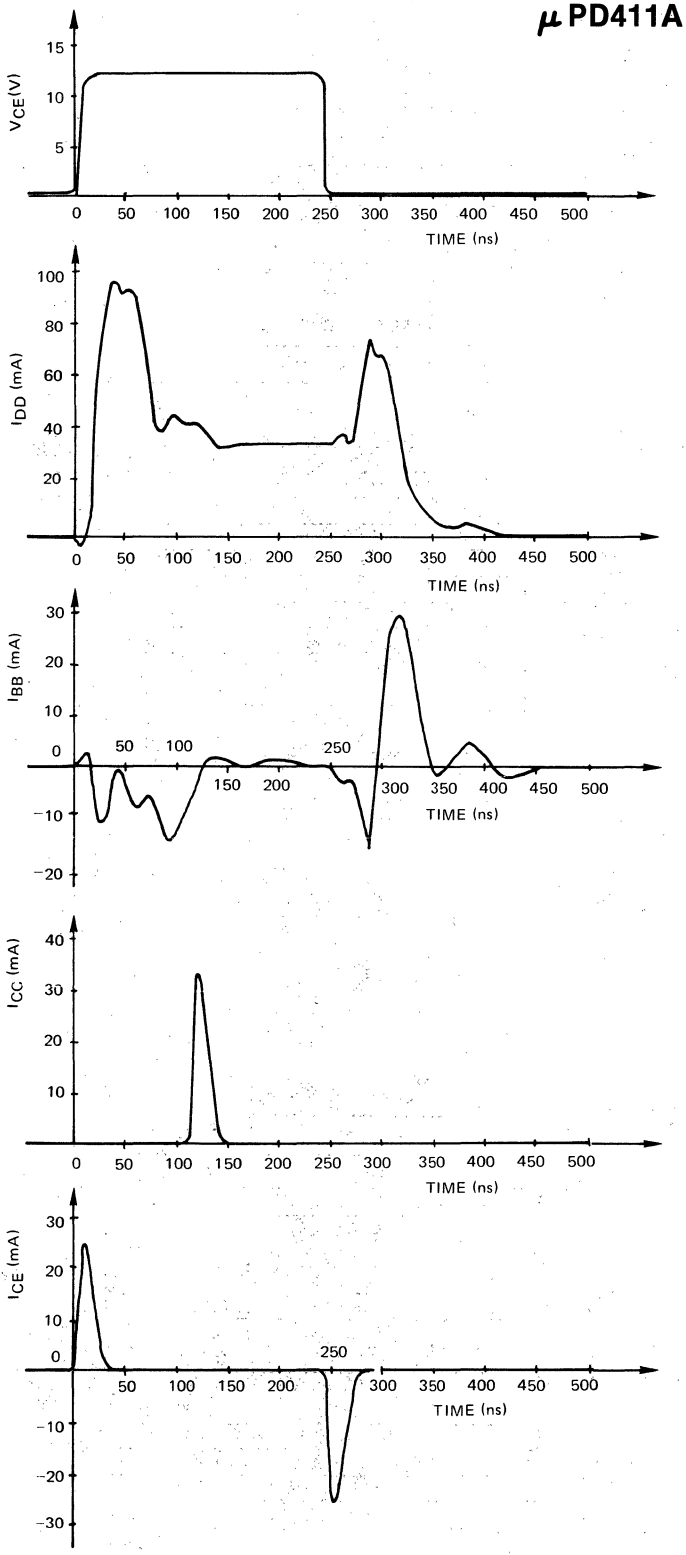
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$

Typical power dissipation for each product is shown below.

	mW (TYP.)	CONDITIONS
μPD411A-E	300 mW	T_a = 25°C, t_{cy} = 800 ns, t_{CE} = 380 ns
μPD411A	460 mW	T_a = 25°C, t_{cy} = 470 ns, t_{CE} = 300 ns
μPD411A-1	460 mW	T_a = 25°C, t_{cy} = 430 ns, t_{CE} = 260 ns
μPD411A-2	460 mW	T_a = 25°C, t_{cy} = 400 ns, t_{CE} = 230 ns

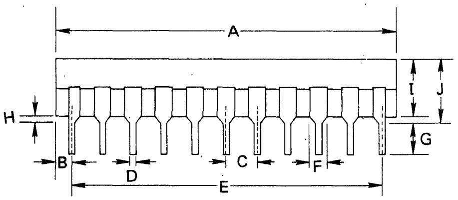
See curve above for power dissipation versus cycle time.

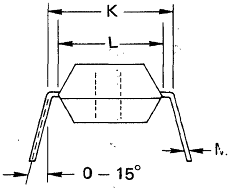
CURRENT WAVEFORMS ①



Note: ① V_{DD} = 12V, V_{BB} = −5.0V, V_{CC} = 5.0V

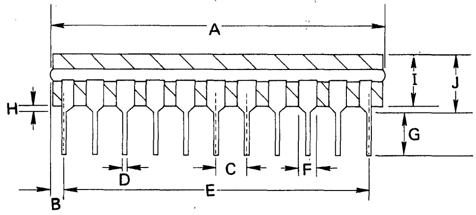
PACKAGE OUTLINE
μPD411AC/D

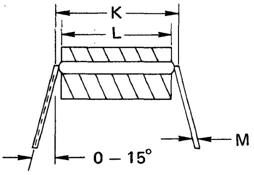




μPD411AC (Plastic)

ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$





μPD411AD (Cerdip)

ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

NEC Microcomputers, Inc.

NEC

µPD416
µPD416-1
µPD416-2
µPD416-3
µPD416-5

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC µPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The µPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

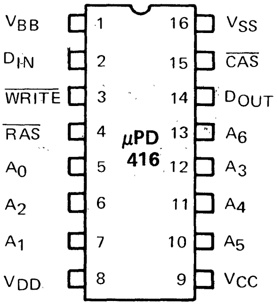
Multiplexed address inputs permit the µPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density — 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 20 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE
µPD416	300 ns	510 ns	575 ns
µPD416-1	250 ns	410 ns	465 ns
µPD416-2	200 ns	375 ns	375 ns
µPD416-3	150 ns	375 ns	375 ns
µPD416-5	120 ns	320 ns	320 ns

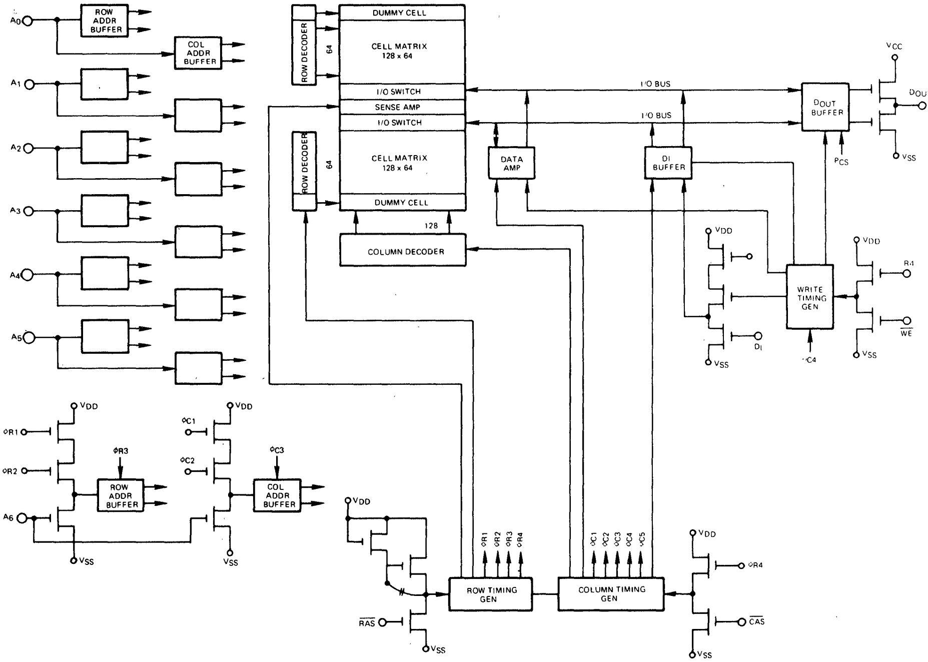
PIN CONFIGURATION



A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

Rev/1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

DC CHARACTERISTICS

T_a = 0°C to +70°C①, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	②
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	② ③
Supply Voltage	V_{SS}	0	0	0	V	②
Supply Voltage	V_{BB}	− 4.5	−5.0	−5.5	V	②
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	②
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	②
Input Low (Logic 0) Voltage, all inputs	V_{IL}	− 1.0		0.8	V	②
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ Min. ④
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{DD} Current — All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$; t_{RC} = 375 ns ④
Refresh V_{DD} Current — μPD416-5	I_{DD3}			27	mA	
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = 225 ns ④
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = 375 ns ⑤
Standby V_{CC} Current	I_{CC2}	-10		10	μA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$, t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, t_{PC} 225 ns ⑤
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$, t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = −5 mA ③
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: ① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

② All voltages referenced to V_{SS}.

③ Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

④ I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

⑤ I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

DERATING CURVES

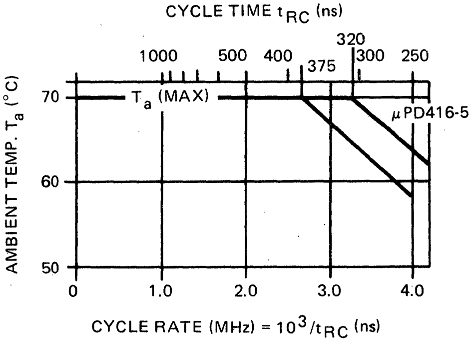


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz ($t_{CYC} < 375$ ns) is determined by T_a (max) [°C] = 70 – 9.0 x (cycle rate [MHz] –2.66). For μPD416-5, it is T_a (max) [°C] = 70 – 9.0 (cycle rate [MHz] – 3.125).

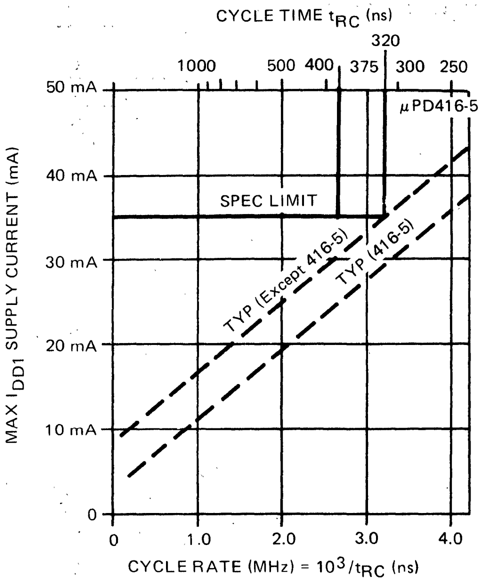


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

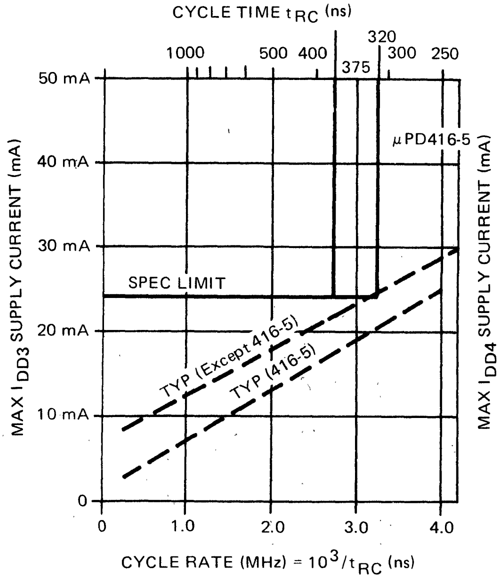


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

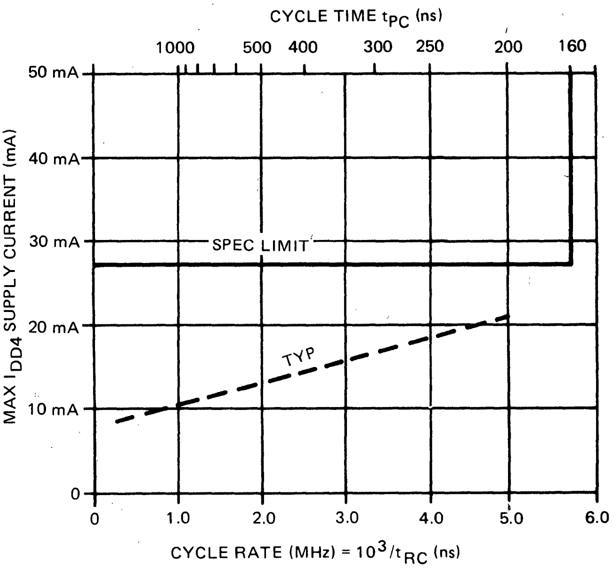


FIGURE 4

Maximum I_{DD4} versus cycle rate for device operation in page mode.

AC CHARACTERISTICS

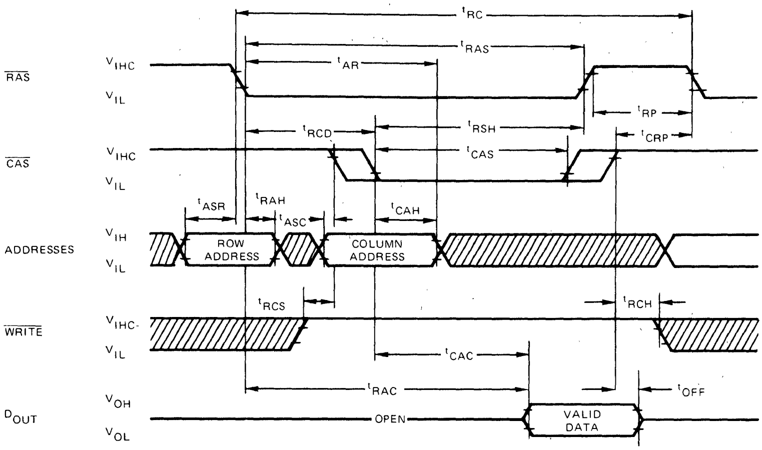
$T_a = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 10\%$, $V_{CC} = +5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		µPD416		µPD416-1		µPD416-2		µPD416-3		µPD416-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	510		410		375		375		320		ns	③
Read-write cycle time	t_{RWC}	575		465		375		375		320		ns	③
Page mode cycle time	t_{PC}	330		275		225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		165		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	60	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		150		120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		165		135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		−20		−20		0		ns	
Row address set-up time	t_{ASR}	0		0		0		0		0		ns	
Row address hold time	t_{RAH}	40		35		25		20		15		ns	
Column address set-up time	t_{ASC}	−10		−10		−10		−10		−10		ns	
Column address hold time	t_{CAH}	90		75		55		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		80		ns	
Write command pulse width	t_{WP}	90		75		55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		100		80		60		60		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		100		80		60		60		ns	
Data-in set-up time	t_{DS}	0		0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		80		ns	
CAS precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		60		ns	
Refresh period	t_{REF}		2		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−20		−20		−20		−20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	140		125		95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	240		200		160		120		120		ns	⑩

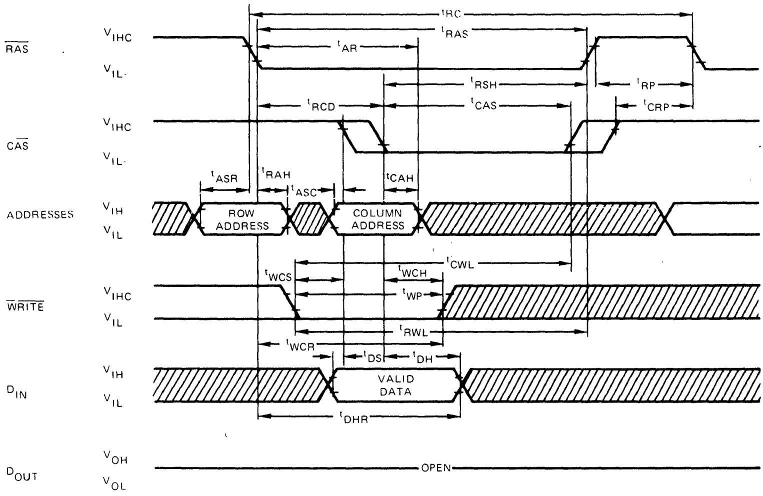
Notes:
① AC measurements assume $t_T = 5$ ns.
② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_a \leq 70°C$) is assured.
④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).
⑥ Measured with a load equivalent to 2 TTL loads and 100 pF
⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

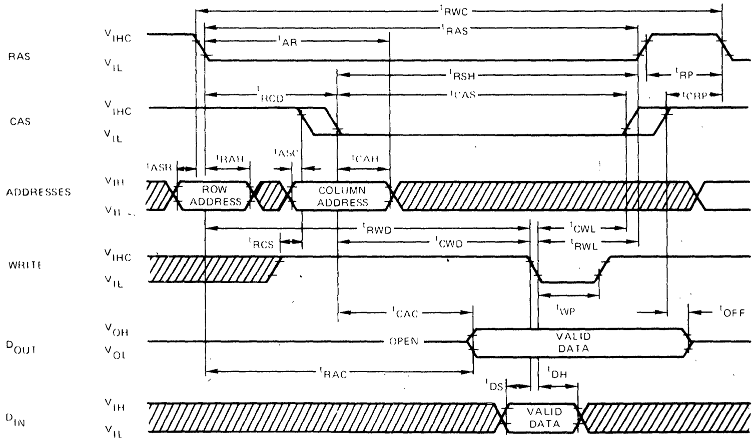
READ CYCLE



WRITE CYCLE

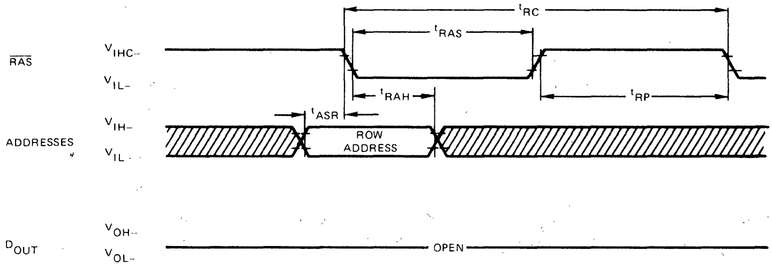


READ-WRITE/READ-MODIFY–WRITE CYCLE



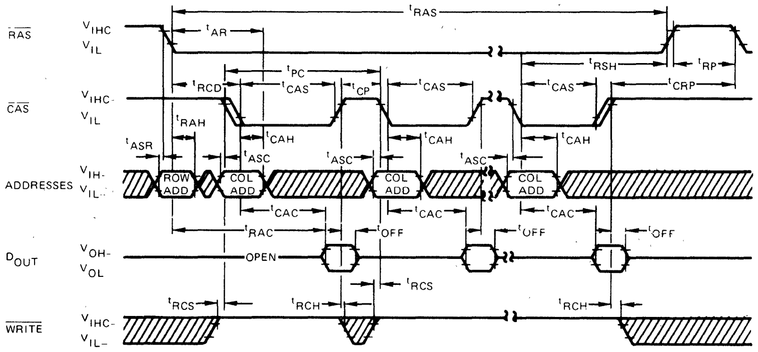
TIMING WAVEFORMS (CONT.)

"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE

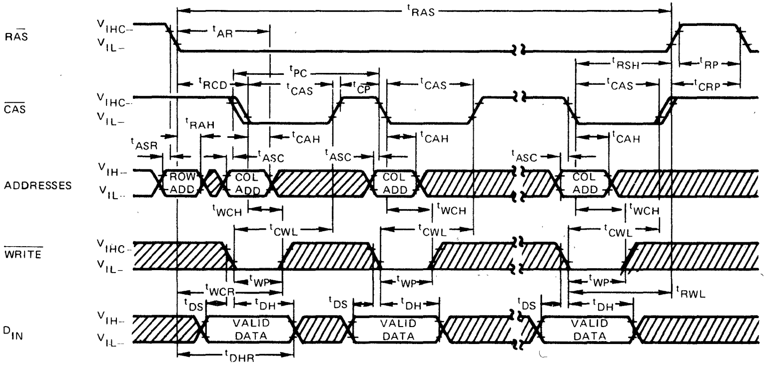


Note $\overline{\text{CAS}}$ · V_{IHC}, $\overline{\text{WRITE}}$ = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{\text{RAS}}$), and the Column Address Strobe ($\overline{\text{CAS}}$). The 7 bit row address is first applied and $\overline{\text{RAS}}$ is then brought low. After the $\overline{\text{RAS}}$ hold time has elapsed, the 7 bit column address is applied and $\overline{\text{CAS}}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{\text{CAS}}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{\text{CAS}}$ instead of $\overline{\text{RAS}}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{\text{WRITE}}$ or $\overline{\text{CAS}}$, whichever occurs later. If $\overline{\text{WRITE}}$ is active before $\overline{\text{CAS}}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{\text{CAS}}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{\text{RAS}}$ and strobing the new column addresses with $\overline{\text{CAS}}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{\text{RAS}}$ only" cycles can be used for simple refreshing operation.

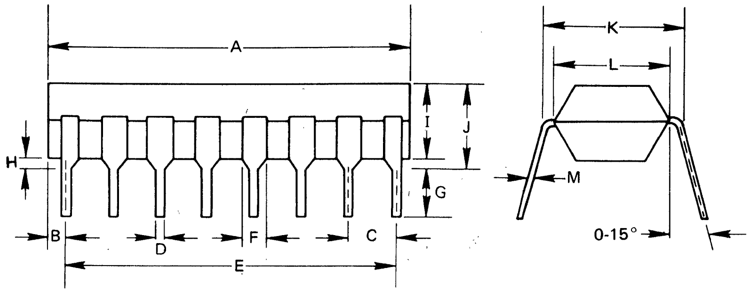
CHIP SELECTION

Either $\overline{\text{RAS}}$ and/or $\overline{\text{CAS}}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

POWER SEQUENCING

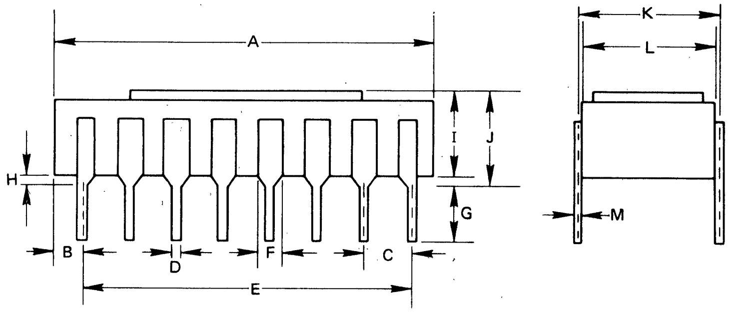
In order to assure long term reliability, V_{BB} should be applied first during power up and removed last during power down.

PACKAGE OUTLINE
μPD416C/D



μPD416C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPD416D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

NEC Microcomputers, Inc.

NEC

μPD2101AL
μPD2101AL-2
μPD2010AL-4

1024 BIT (256 X 4) STATIC MOS RAM WITH SEPARATE I/O

DESCRIPTION

The μPD2101AL is a 256 word by 4 bit static random access memory requiring no clocks or refreshing. It features high speed, low cost, and simplicity of interfacing.

It is directly TTL compatible in all respects; inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bidirectional logic in a common I/O system. Output data is the same polarity as input data, and readout is non-destructive.

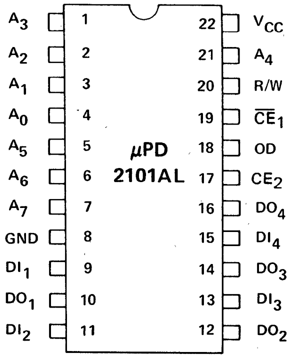
The μPD2101AL family of devices offers access times from 450 ns to 250 ns with a typical standby mode power dissipation of only 36 mW.

The use of NEC's N-channel silicon gate MOS process, with its excellent protection from contamination, permits the use of a low cost 22 pin plastic package in providing a high performance, high reliability MOS circuit at a most cost effective price level. The μPD2101AL is pin-compatible with the μPD5101 CMOS static RAM.

FEATURES

- 256 x 4 Organizations to Meet Needs for Small System Memories
- Access Time — 250 to 450 nsec max
- Directly TTL Compatible — All Inputs and Output
- Static MOS — No Clocks or Refreshing Required
- Simple Memory Expansion — Chip Enable Input
- Low Standby Power — 36 mW typ.
- Low Cost Packaging — 22 Pin Plastic Dual-In-Line Configuration
- Low Operating Power
- Three-State Output — OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

PIN CONFIGURATION



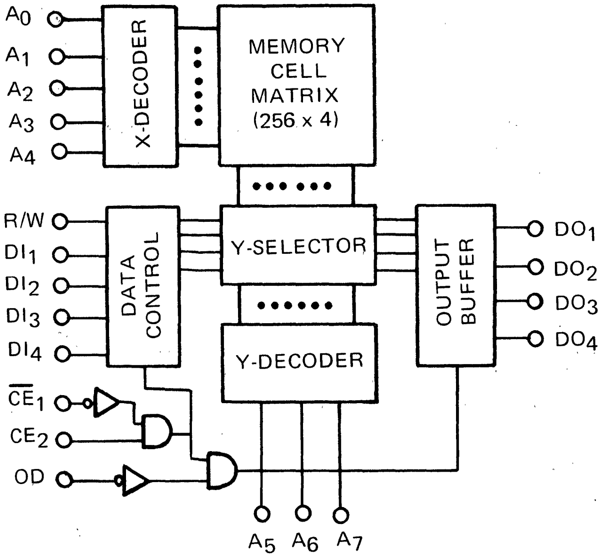
PIN NAMES

DI_1–DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0–A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1–DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

OPERATION MODES

$\overline{CE}_1$	CE_2	OD	CHIP	OUTPUT MODE
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			No-Selected	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Output High Voltage	V_{OH}	+2.4			V	$I_{OH} = -100\ \mu A$
Output Low Voltage	V_{OL}			+0.4	V	$I_{OL} = +2.1$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	$V_I = 0V$
Output Leakage Current High	I_{LOH}			+10	μA	$V_O = +2.4V$ to V_{CC} $\overline{CE}_1 = +2.0V$
Output Leakage Current Low	I_{LOL}			−10	μA	$V_O = +0.4V$ $\overline{CE}_1 = +2.0V$
Power Supply Current	I_{CC1}			+60	mA	$V_I = +5.25V$ $I_O = 0$ mA $T_a = +25°C$
Power Supply Current	I_{CC2}			+70	mA	$V_I = +5.25V$ $I_O = 0$ mA $T_a = -10°C$ to $+70°C$

AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			180			150			130	ns
Output Disable to Output	t_{OD}			150			130			120	ns
Data Output to High Z State	t_{DF}*	0		130	0		115	0		100	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

*t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.

WRITE CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write Cycle Time	t_{WC}	450			350			250			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	180			150			130			ns
Data Setup Time	t_{DW}	180			150			130			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	160			130			120			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			10			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY CHARACTERISTICS

$T_a = -10°C$ to $+70°C$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.①	MAX.		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby	V_{CES}	2.0			V	$2.0V \leq V_{PD} \leq 5.25V$
		V_{PD}			V	$1.5V \leq V_{PD} < 2.0V$
Standby Current Drain	I_{PD1}		24	36	mA	All Inputs $= V_{PD1} = 1.5V$
Standby Current Drain	I_{PD2}		30	45	mA	All Inputs $= V_{PD2} = 2.0V$
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC}②			ns	

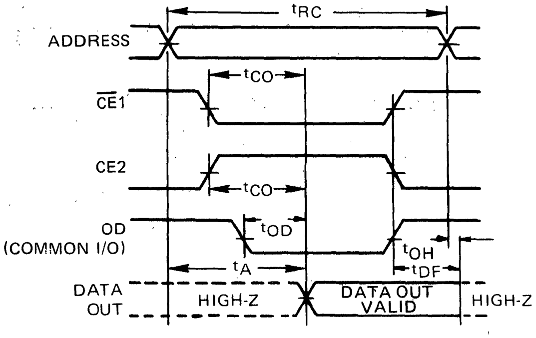
Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage.
② $t_R = t_{RC}$ (Read Cycle Time).

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			8	pf	$V_I = 0V$
Output Capacitance	C_{OUT}			12	pf	$V_O = 0V$

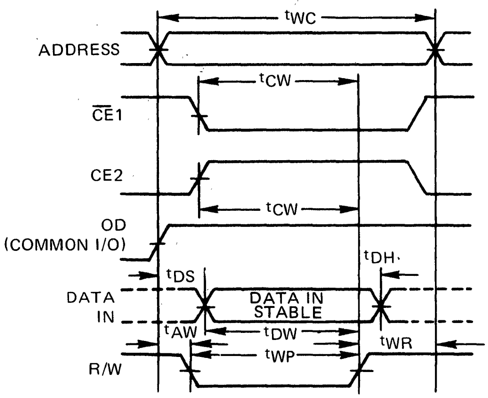
TIMING WAVEFORMS

READ CYCLE



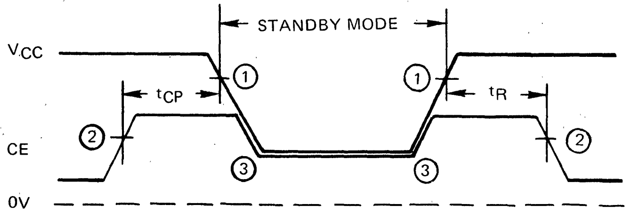
Notes: ① OD should be tied low for separate I/O operation.
② R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS

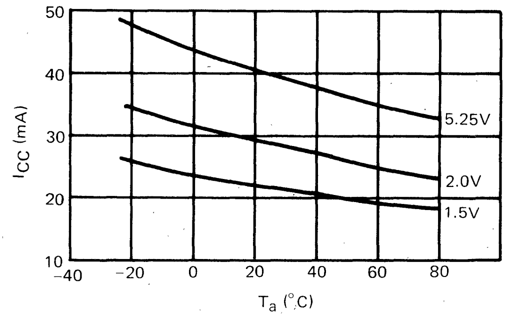


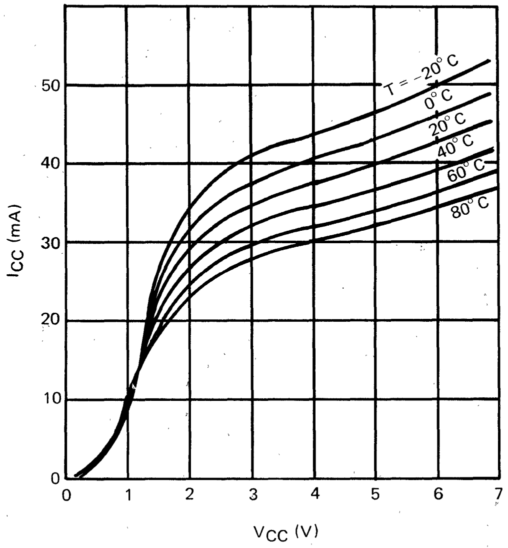
Notes: ① 4.75V
② 2.0V
③ 1.5V

AC CONDITIONS OF TEST

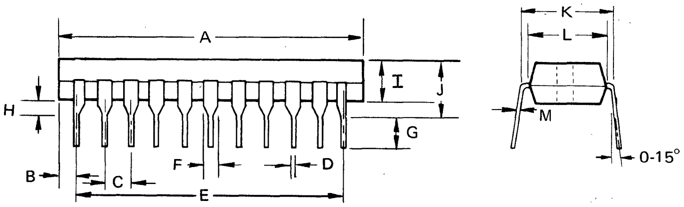
Input Pulse Levels	+0.8V to +2.0V
Input Pulse Rise and Fall Times	20 ns
Timing Measurement Reference Level	1.5V
Output Load	1 TTL + 100 pF

TYPICAL OPERATING CHARACTERISTICS


I_{CC} VS T_a


I_{CC} VS V_{CC}

PACKAGE OUTLINE μPD2101ALC



ITEM	MILLIMETERS	INCHES
A	28.0 MAX.	1.10 MAX.
B	1.4 MAX	0.025
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.7 MAX.	0.18 MAX.
J	5.2 MAX.	0.20 MAX.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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μPD2102AL
μPD2102AL-2
μPD2102AL-4

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD2102AL is a 1024 words by one bit static Random Access Memory requiring no clocks or refreshing. A family of devices with maximum access times ranging from 250 ns to 450 ns meet the requirements of microcomputer memory applications where speed, low cost and easy interfacing are prime design objectives.

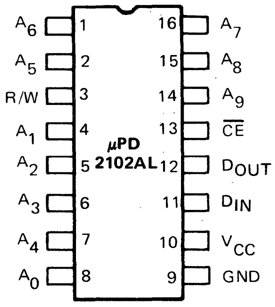
All μPD2102AL inputs and outputs are TTL compatible. A single chip-enable ($\overline{CE}$) pin is provided for selection of an individual device in systems with OR-tied outputs. Output data is the same polarity as input data and is nondestructively read out. Only a single +5 volt supply is required. In standby mode, with the supply lowered to 1.5 volts, power dissipation is reduced to 42 mW max.

The μPD2102AL family is fabricated using NEC's N-channel MOS silicon gate process, providing excellent contamination protection. This process permits the use of a low cost plastic package (16 pin) and enables high performance, highly reliable MOS circuits to be produced.

FEATURES

- Access Time – μPD2102AL-2 – 250 ns Max
  μPD2102AL – 350 ns Max
  μPD2102AL-4 – 450 ns Max
- Single +5 Volts Supply Voltage
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Low Power – Typically 150 mW
- Low Standby Power – 42 mW max
- Three-State Output – OR-TIE Capability
- Simple Memory Expansion – Chip Enable Input
- Fully Decoded – On Chip Address Decode
- Inputs Protected – All Inputs have Protection against Static Charge
- Low Cost Packaging – 16 Pin Plastic Dual-In-Line Configuration

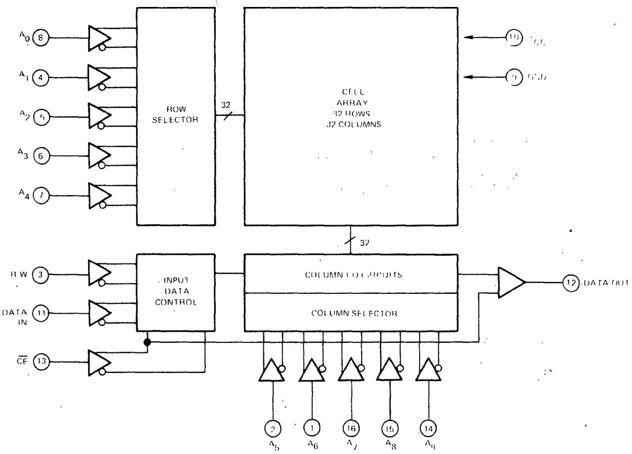
PIN CONFIGURATION



PIN NAMES

$A_0 - A_9$	Address Inputs
R/W	Read/Write
$\overline{CE}$	Chip Enable
V_{CC}	Power (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . −10°C to 70°C

Storage Temperature. . . . . −65°C to +125°C

Voltage On Any Pin . . . . −0.5 to +7 Volts ①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP ①	MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}			±10	μA	V_{IN} = 0 to 5.25V
I/O Leakage Current	I_{LOH}			+5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = +2.4V to V_{CC}
I/O Leakage Current	I_{LOL}			−10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
Power Supply Current	I_{CC1}		30	70	mA	All Inputs = 5.25V, Data Out Open
Input "Low" Voltage	V_{IL}	−0.5		+0.8	V	
Input "High" Voltage	V_{IH}	20		V_{CC}	V	
Output "Low" Voltage	V_{OL}			+0.4	V	I_{OL} = 2.1 mA
Output "High"	V_{OH}	2.4			V	I_{OH} = −100 μA

Note: ① Typical values are for T_a = 25°C and nominal supply voltage

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		3	5	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}		7	10	pf	V_{OUT} = 0V

AC CHARACTERISTICS

READ CYCLE

T_a = −10°C to +70°C; V_{CC} = +5V ±5% unless otherwise noted

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		2102AL-4		2102AL		2102AL-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle	t_{RC}	450		350		250		ns	$t_T = t_r = t_f$ = 100 ns C_L = 100 pF Load = 1 TTL Gate V_{ref} = 2.0 or 0.8V
Access Time	t_A		450		350		250	ns	
Chip Enable to Output Time	t_{CO}		230		180		130	ns	
Previous Read Data Valid in Respect to Address	t_{OH1}	40		40		40		ns	
Previous Read Data Valid in Respect to Chip Enable	t_{OH2}	0		0		0		ns	

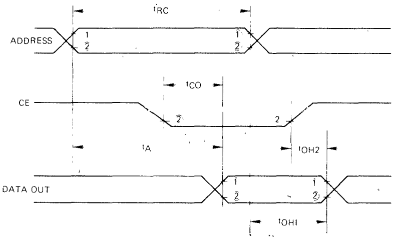
WRITE CYCLE

T_a = −10°C to +70°C; V_{CC} = +5V ±5% unless otherwise noted

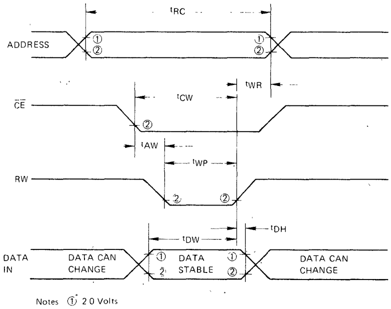
PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		2102AL-4		2102AL		2102AL-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Write Cycle	t_{WC}	450		350		250		ns	$t_T = t_r = t_f$ = 100 ns C_L = 100 pF Load = 1 TTL Gate V_{ref} = 2.0 or 0.8V
Address to Write Setup Time	t_{AW}	20		20		20		ns	
Write Pulse Width	t_{WP}	300		250		180		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Data Setup Time	t_{DW}	300		250		180		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
Chip Enable to Write Setup Time	t_{CW}	300		250		180		ns	

TIMING WAVEFORMS

READ CYCLE



WRITE CYCLE



Notes ① 2.0 Volts
② 0.8 Volts

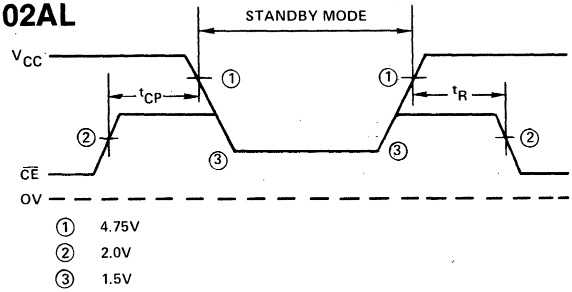
STANDBY CHARACTERISTICS

T_a 0 to +70 C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}$ Bias in Standby	V_{CES}	2.0			V	+2.0V V_{PD} +5.25V
		V_{PD}			V	+1.5V V_{PD} +2.0V
Standby Current Drain	I_{PD1}		14	28	mA	All Inputs, V_{PD1} +1.5
Standby Current Drain	I_{PD2}		18	38	mA	All Inputs, V_{PD2} +2.0V
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC} ①			ns	

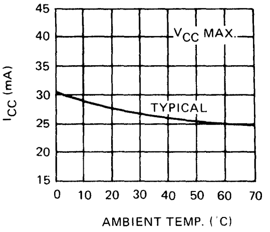
① t_{RC} Read Cycle Time

STANDBY MODE TIMING WAVEFORM

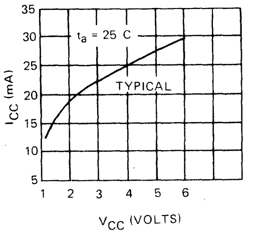


TYPICAL CHARACTERISTICS

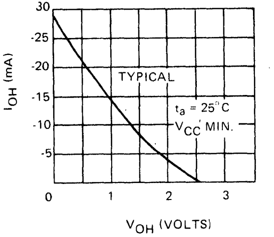
POWER SUPPLY CURRENT VS AMBIENT TEMPERATURE



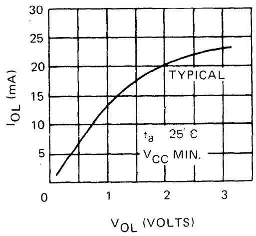
POWER SUPPLY CURRENT VS SUPPLY VOLTAGE



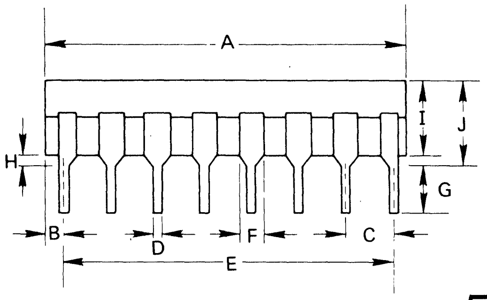
OUTPUT SOURCE CURRENT VS OUTPUT VOLTAGE

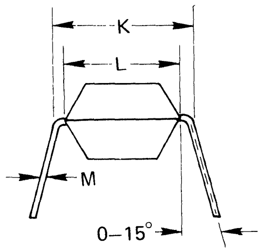


OUTPUT SINK CURRENT VS OUTPUT VOLTAGE



PACKAGE OUTLINE μPD2102ALC





ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25\,^{+0.10}_{-0.05}$	0.01

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μPD2111AL
μPD2111AL-2
μPD2111AL-4

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

DESCRIPTION

The μPD2111AL is a 256 words by 4 bits static random access memory fabricated with N-channel MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

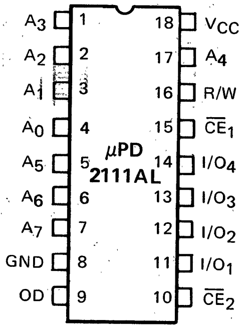
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

All members in the μPD2111AL family feature a low standby power mode with the supply voltage being reduced to +1.5V.

FEATURES

- 256 Words x 4 Bits Organization
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Access Time — 250 ns to 450 ns max.
- Simple Memory Expansion — Chip Enable Inputs
- Fully Decoded — On Chip Address Decode
- Inputs Protected — All Inputs have Protection Against Static Charge
- Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration
- Three-State Output — OR-Tie Capability
- Low Standby Power

PIN CONFIGURATION



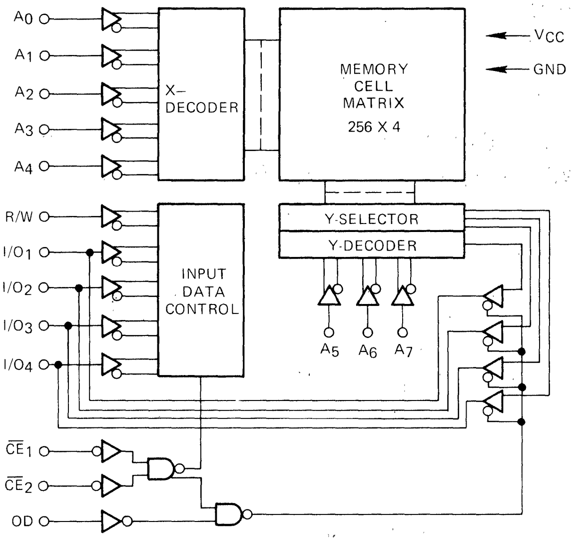
PIN NAMES

A_0 - A_7	Address Inputs
OD	Output Disable
R/W	Read/Write Input
$\overline{CE}_1$	Chip Enable 1
$\overline{CE}_2$	Chip Enable 2
I/O_1 - I/O_4	Data Input/Output

OPERATION MODES

CE_1	CE_2	OD	Chip Output Status	
0	1	0	Selected	Data Output
0	1	1		High Z State
Others			Unselected	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +125°C
All Output Voltages	–0.5 to +7 Volts
All Input Voltages	–0.5 to +7 Volts
Supply Voltage V_{CC}	–0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

T_a = -10 to +70°C; V_{CC} = +5V ± 5%

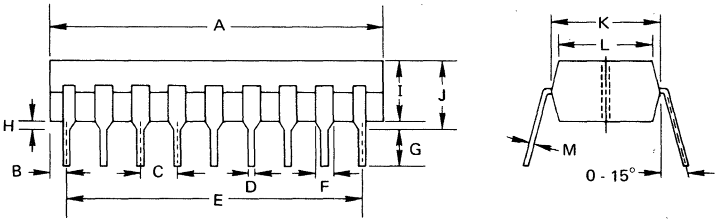
PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP	MAX		
Input High Voltage		V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage		V_{IL}	–0.5		+0.8	V	
Output High Voltage	2111AL-4	V_{OH}	+2.4			V	I_{OH} = –150 μA
	2111AL		+2.4			V	I_{OH} = –200 μA
	2111AL-2						
Output Low Voltage		V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High		I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low		I_{LIL}			–10	μA	V_I = OV
Output Leakage Current High		I_{LOH}			+5	μA	V_O = +2.4V to V_{CC} $\overline{CE}$ = +2.0V
Output Leakage Current Low		I_{LOL}			–10	μA	V_O = +0.4V $\overline{CE}$ = +2.0V
Power Supply Current	2111AL-4	I_{CC1}			50	mA	V_I = +5.25V
	2111AL				55	mA	I_O = 0 mA
	2111AL-2						T_a = +25°C
Power Supply Current	2111AL-4	I_{CC2}			60	mA	V_I = +5.25V
	2111AL				65	mA	I_O = 0 mA
	2111AL-2						T_a = –10 to +70°C

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			8	pf	$V_I = 0V$
Output Capacitance	C_{OUT}			12	pf	$V_O = 0V$

PACKAGE OUTLINE
μPD2111ALC



ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

NEC Microcomputers, Inc.

NEC

μPD410
μPD410-1
μPD410-2
μPD410-3
μPD410-5

4096 BIT HIGH SPEED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD410 is a very high speed 4K bit static random access memory. It is organized as 4096 words by 1 bit per word and fabricated using N channel silicon gate MOS technology.

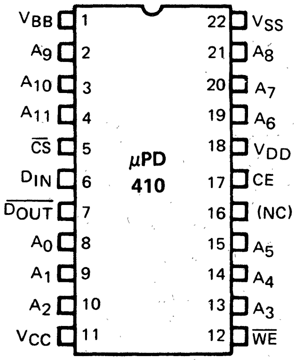
All signals to the device are TTL compatible except for Chip Enable which is standard +12 Volt MOS level.

Circuit operation starts with the rising edge of CE. Data is latched and valid until falling edge of CE. Address and Chip Select signals are latched on-chip to simplify system timing requirements.

FEATURES

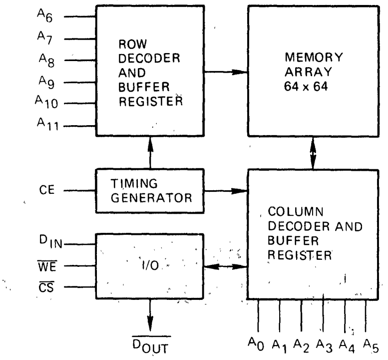
- 4096 Words x 1 Bit Organization
- Fully Decoded
- TTL Compatible (except CE)
- High Speed-Access Time: 80 ns max.
- Cycle Time: 220 ns min.
- Static Operation — No Refresh Required
- Standby Power: 75 mW max.
- Active Power: 470 mW typ.
- Supply Voltages: V_{DD} = +12V, V_{CC} = +5V, V_{BB} = -5V
- Address Registers on the Chip
- Three State Output
- Standard 22 Pin Ceramic Dual-in-Line Package
- Pin Compatible with μPD411 and Other 4K Dynamic RAMs

PIN CONFIGURATION



Rev/2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.3 to +20 Volts①
All Input Voltages	-0.3 to +20 Volts①
Supply Voltage V_{DD}	-0.3 to +20 Volts①
Supply Voltage V_{CC}	-0.3 to +20 Volts①
Supply Voltage V_{SS}	-0.3 to +20 Volts①
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}		10	μA	V_{IN} = V_{IL}MIN to V_{IH}MAX
CE Input Leakage Current	I_{LC}		10	μA	V_{IN} = V_{ILC}MIN to V_{IHC}MAX
Output Leakage Current	I_{LO}		10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DDOFF}		200	μA	CE = -1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DDON}		20	mA	CE = V_{IHC}
Average V_{DD} Current μPD410	I_{DDAV}		24	mA	Minimum Cycle Time
μPD410-1	I_{DDAV}		32	mA	
μPD410-2	I_{DDAV}		45	mA	
μPD410-3	I_{DDAV}		45	mA	
μPD410-5	I_{DDAV}		45	mA	
V_{BB} Supply Current	I_{BB}		100	μA	
V_{CC} Supply Current during CE off	I_{CCOFF}		15	mA	$\overline{CE}$ = V_{ILC} or $\overline{CS}$ = V_{IH}
Average V_{CC} Current	I_{CCAV}		21	mA	D_{OUT} = No load
Input Low Voltage	V_{IL}	-1.0	0.6	V	
Input High Voltage	V_{IH}	2.4	V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	-1.0	0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}-1	V_{DD}+1	V	
Output Low Voltage	V_{OL}	0	0.4	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	I_{OH} = 2.0 mA

CAPACITANCE

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

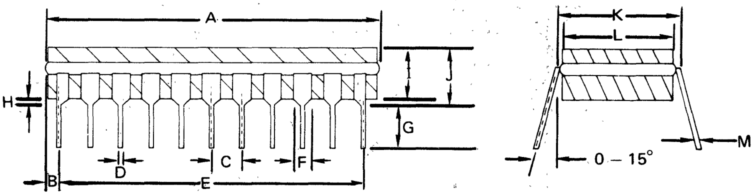
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}		4	6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}		4	6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}		5	7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}		8	10	pf	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pf	V_{IN} = V_{SS}

AC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{DD} = 12V \pm 5\%$; $V_{CC} = 5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		410		410-1		410-2		410-3		410-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ, WRITE AND READ-MODIFY-WRITE													
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		ns	
Address Hold Time	t_{AH}	90		70		50		50		50		ns	
CE Off Time	t_{CC}	190		140		90		90		90		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	ns	
CE off to Output High Impedance State	t_{CF}	0	90	0	90	0	90	0	90	0	90	ns	
READ													
Cycle Time	t_{CY}	440		330		220		220		220		ns	t_T - 10 ns
CE on Time	t_{CE}	230	2000	170	2000	110	2000	110	2000	110	2000	ns	
CE Output Delay	t_{CO}		190		140		90		80		70	ns	Load = 50 pF + 1TTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}		200		150		100		90		80	ns	$t_{ACC} = t_{AC} + t_{CO} + t_T$
CE to $\overline{WE}$	t_{WL}	20		20		20		20		20		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		ns	
WRITE													
Cycle Time	t_{CY}	440		330		220		220		220		ns	t_T = 10 ns
CE on Time	t_{CE}	230	2000	170	2000	110	2000	110	2000	110	2000	ns	
$\overline{WE}$ to CE off	t_W	130		100		70		70		70		ns	
CE to $\overline{WE}$	t_{CW}	130		100		70		70		70		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	60		40		20		20		20		ns	
$\overline{WE}$ Pulse Width	t_{WP}	130		100		70		70		70		ns	
READ-MODIFY-WRITE													
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	560		420		280		280		280		ns	t_T 10 ns
CE Width During RMW	t_{CRW}	350	2000	260	2000	170	2000	170	2000	170	2000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		ns	
$\overline{WE}$ to CE off	t_W	130		100		70		70		70		ns	
$\overline{WE}$ Pulse Width	t_{WP}	130		100		70		70		70		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	60		40		20		20		20		ns	
CE to Output Delay	t_{CO}		190		140		90		80		70	ns	Load = 50 pF + 1TTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}		200		150		100		90		80		$t_{ACC} = t_{AC} + t_{CO} + t_T$

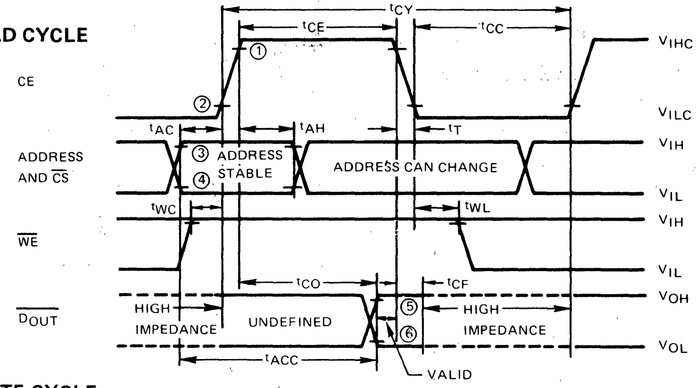
PACKAGE OUTLINE
μPD410D



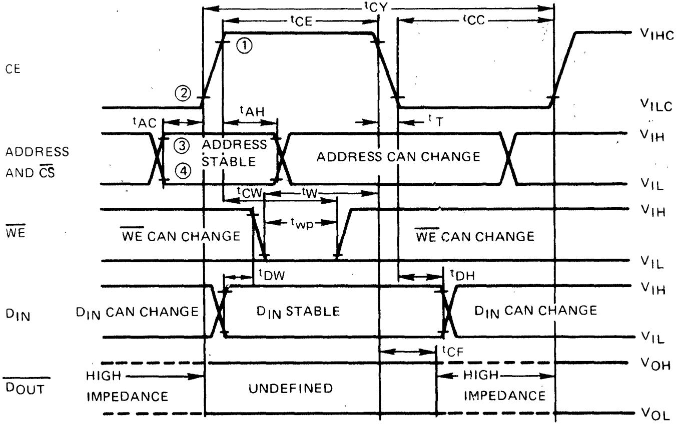
ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

TIMING WAVEFORMS

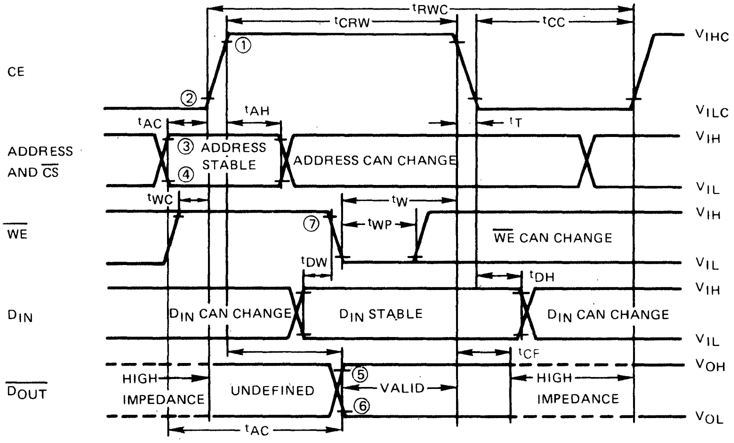
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:
① $V_{DD} - 2V$ is the reference level for measuring timing of CE.
② $V_{SS} + 2V$ is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ $V_{SS} + 2.0V$ is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑥ $V_{SS} + 0.8V$ is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

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NEC

μPD2114L
μPD2114L-1
μPD2114L-2
μPD2114L-3
μPD2114L-5

4096 BIT (1024 × 4 BITS) STATIC RAM

DESCRIPTION

The NEC μPD2114L is a 4096 bit static Random Access Memory organized as 1024 words by 4 bits using N-channel Silicon-gate MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, and therefore requires no clocks or refreshing to operate and simplify system design. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

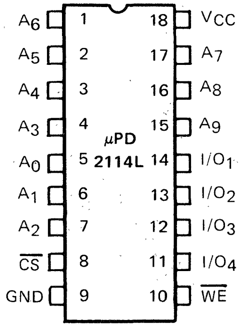
The μPD2114L is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The μPD2114L is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-Tied.

FEATURES

- Access Time: Selection from 150-450 ns
- Single +5 Volt Supply
- Directly TTL Compatible – All Inputs and Outputs
- Completely Static – No Clock or Timing Strobe Required
- Low Operating Power – Typically 0.06 mW/Bit
- Identical Cycle and Access Times
- Common Data Input and Output using Three-State Output
- High Density 18-pin Plastic and Ceramic Packages
- Replacement for 2114L and Equivalent Devices

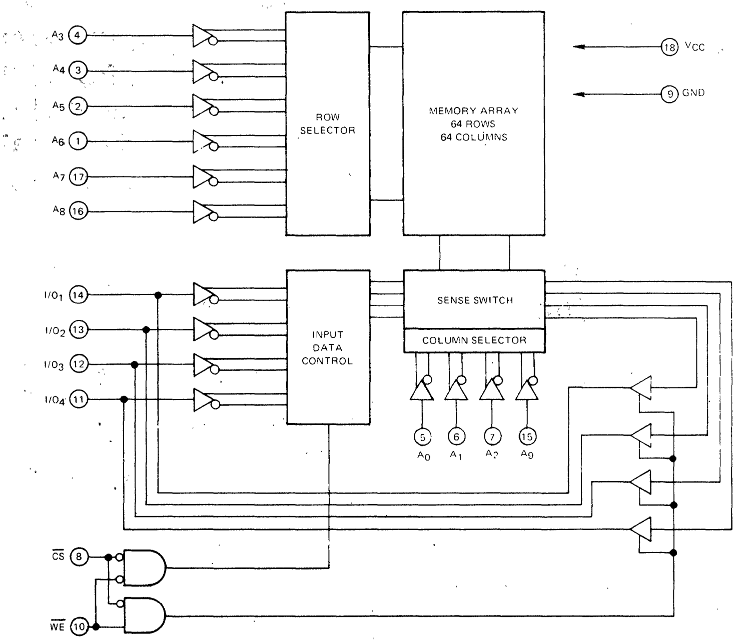
PIN CONFIGURATION



PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin	−0.5 to +7 Volts ①
Power Dissipation	1 Watt

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C; f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			12	pf	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}			5	pf	V_{IN} = 0V

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = 0 to 5.5V
I/O Leakage Current	I_{LO}			10	μA	$\overline{CS}$ = 2V, $V_{I/O}$ = 0.4V to V_{CC}
Power Supply Current	I_{CC1}			65	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_a = 25°C
Power Supply Current	I_{CC2}			70	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_a = 0°C
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Current	I_{OL}	3.2			mA	V_{OL} = 0.4V
Output High Current	I_{OH}			−1.0	mA	V_{OH} = 2.4V, V_{CC} = 4.75V V_{OH} = 2.2V, V_{CC} = 4.5V

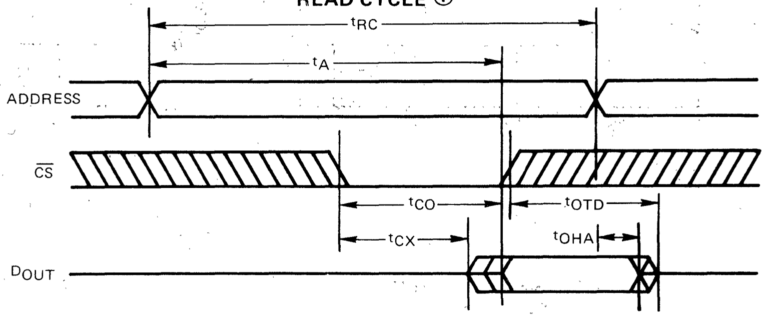
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

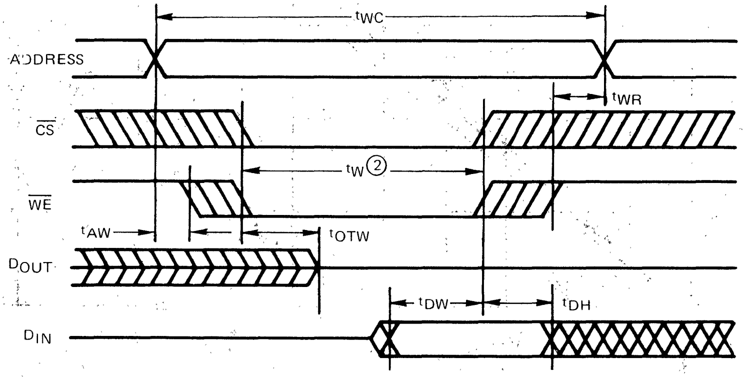
PARAMETER	SYMBOL	LIMITS 2114L MIN	2114L MAX	2114L-1 MIN	2114L-1 MAX	2114L-2 MIN	2114L-2 MAX	2114L-3 MIN	2114L-3 MAX	2114L-5 MIN	2114L-5 MAX	UNIT	TEST CONDITIONS
READ CYCLE													
Read Cycle Time	t_{RC}	450		300		250		200		150		ns	$t_T = t_r = t_f = 10$ ns
Access Time	t_A		450		300		250		200		150	ns	$C_L = 100$ pF
Chip Selection to Output Valid	t_{CO}		120		100		80		70		60	ns	Load = 1 TTL gate
Chip Selection to Output Active	t_{CX}	20		20		20		20		20		ns	Input Levels = 0.8 and 2.0V
Output 3-State from Deselection	t_{OTD}		100		80		70		60		50	ns	$V_{ref} = 1.5V$
Output Hold from Address Change	t_{OHA}	50		50		50		50		50		ns	
WRITE CYCLE													
Write Cycle Time	t_{WC}	450		300		250		200		150		ns	$t_T = t_r = t_f = 10$ ns
Write Time	t_W	200		150		120		120		80		ns	$C_L = 100$ pF
Write Release Time	t_{WR}	0		0		0		0		0		ns	Load = 1 TTL gate
Output 3-State from Write	t_{OTW}		100		80		70		60		50	ns	Input Levels = 0.8 and 2.0V
Data to Write Time Overlap	t_{DW}	200		150		120		120		80		ns	$V_{ref} = 1.5V$
Data Hold from Write Time	t_{DH}	0		0		0		0		0		ns	
Address to Write Setup Time	t_{AW}	0		0		0		0		0		ns	

TIMING WAVEFORMS

READ CYCLE ①



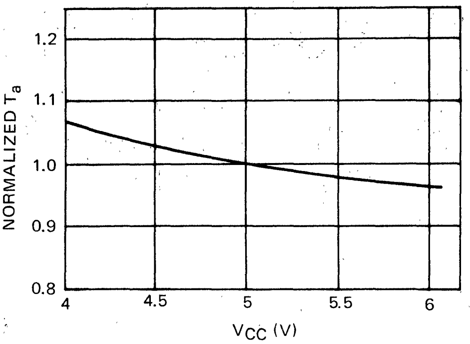
WRITE CYCLE

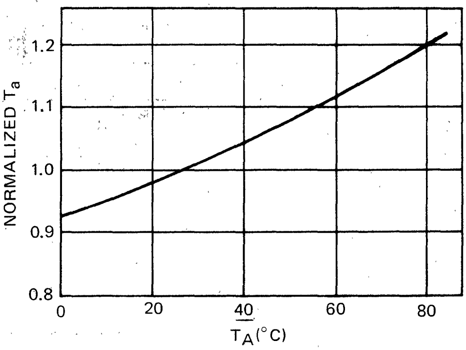


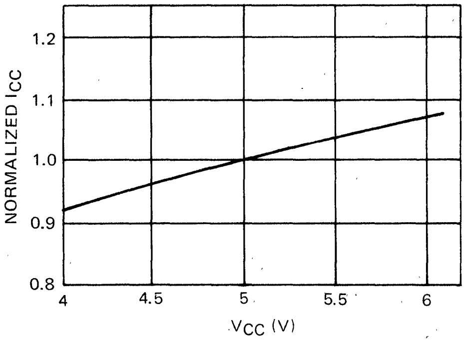
Notes: ① $\overline{WE}$ is high for Read Cycle

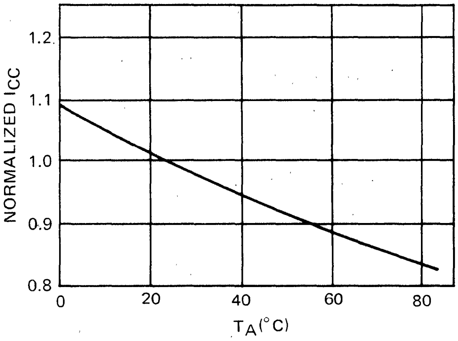
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

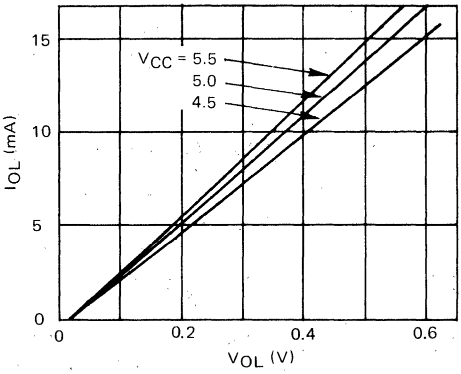
TYPICAL OPERATING CHARACTERISTICS

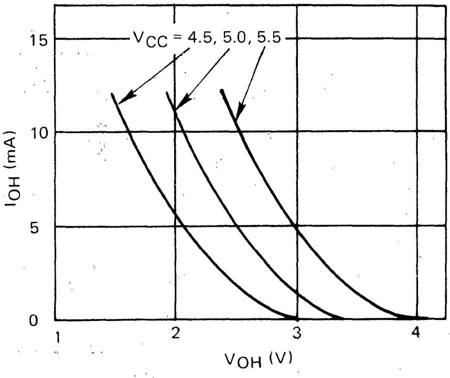

NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE


NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE

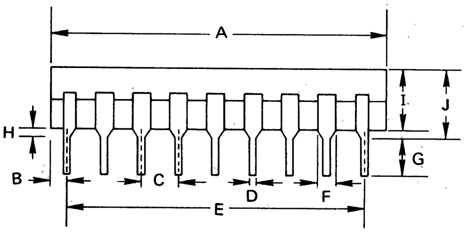

NORMALIZED POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE

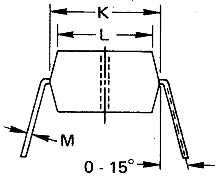

NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE


OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE

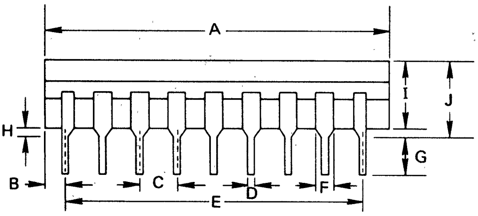
PACKAGE OUTLINES
μPD2114LC/D

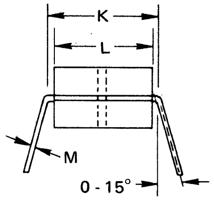




μPD2114LC (Plastic)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01





μPD2114LD (Cerdip)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

NEC

NEC Microcomputers, Inc.

μPD2147
μPD2147-2
μPD2147-3
PRELIMINARY

4096 X 1 BIT STATIC RAM

DESCRIPTION

The μPD2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1 bit using a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with nonclocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high – deselecting the μPD2147 – the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85 percent in larger systems, where the majority of devices are deselected.

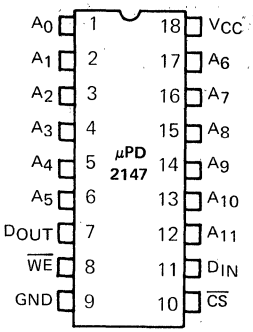
The μPD2147 is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

FEATURES

- Completely Static Memory – No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power-Down
- Directly TTL Compatible – All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Available in Standard 18-Pin Ceramic Package
- Three Performance Ranges:

	ACCESS TIME	ACTIVE CURRENT	STANDBY CURRENT
μPD2147	85 ns	160 mA	20 mA
μPD2147-2	70 ns	160 mA	20 mA
μPD2147-3	55 ns	180 mA	30 mA

PIN CONFIGURATION



PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

NEC Microcomputers, Inc.

NEC

μPD4104-30
μPD4104-32
μPD4104-33
μPD4104-35
μPD4104-36

4096 x 1 STATIC NMOS RAM

DESCRIPTION

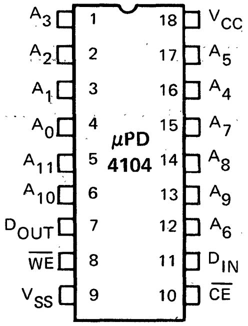
The μPD4104 is a high performance 4K static RAM. Organized as 4096 x 1, it uses a combination of static storage cells with dynamic input/output circuitry to achieve high speed and low power in the same device. Utilizing NMOS technology, the μPD4104 is fully TTL compatible and operates with a single +5V ± 10% supply.

FEATURES

- Fast Access Time – 85 ns (μPD4104-36)
- Very Low Stand-By Power – 28 mW Max.
- Low V_{CC} Data Retention Mode to +3 Volts
- Single +5V ± 10% Supply
- Fully TTL Compatible
- Available in 18 Pin Plastic and Ceramic Dual-in-Line Packages
- 5 Performance Ranges:

			SUPPLY CURRENT	
	ACCESS TIME	R/W CYCLE	ACTIVE	STANDBY
μPD4104-30	300 ns	460 ns	21 mA	5 mA
μPD4104-32	200 ns	310 ns	21 mA	5 mA
μPD4104-33	150 ns	260 ns	40 mA	5 mA
μPD4104-35	120 ns	230 ns	40 mA	5 mA
μPD4104-36	85 ns	180 ns	40 mA	5 mA

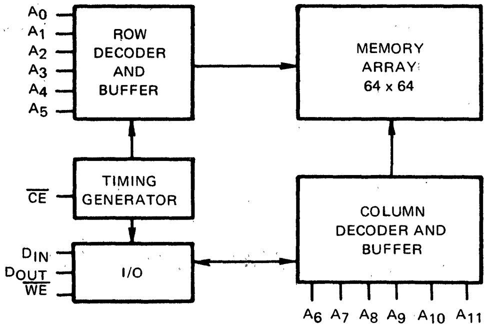
PIN CONFIGURATION



PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{CE}$	Chip Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{SS}	Ground
V_{CC}	Power (+5V)
$\overline{WE}$	Write Enable

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Plastic Package)	−55°C to +125°C
(Ceramic Package)	−65°C to +150°C
Voltage on Any Pin	−1 to +7 Volts ①
Power Dissipation	1 Watt
Short Circuit Output Current	50 mA

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$^*T_a = 25°C$

DC CHARACTERISTICS ①⑥

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER		SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	All Voltages Referenced to V_{SS}
Supply Voltage		V_{SS}	0	0	0	V	
Logic "1" Voltage All Inputs		V_{IH}	2.2		7.0	V	
Logic "0" Voltage All Inputs		V_{IL}	−1.0		0.8	V	
Average V_{CC} Power Supply Current	4104-30, 4104-32	I_{CC1}			21	mA	
	4104-33, 4104-35, 4104-36	I_{CC1}			40	mA	②
Standby V_{CC} Power Supply Current		I_{CC2}			5	mA	③
Input Leakage Current (Any Input)		I_{IL}	−10		10	μA	④
Output Leakage Current		I_{OL}	−10		10	μA	③ ⑤
Output Logic "1" Voltage $I_{OUT} = -500\ \mu A$		V_{OH}	2.4			V	
Output Logic "0" Voltage $I_{OUT} = 5\ mA$		V_{OL}			0.4	V	

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	⑦
Output Capacitance	C_{OUT}		6	7	pF	⑦

Notes: ① All voltages referenced to V_{SS}.

② I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by:

$$I_{CC1}\,[ma] = (5t_p + 13\,(t_C - t_p) + 3420) \div t_C$$

where t_p and t_C are expressed in nanoseconds. Equation is referenced to the −3 device, other devices derate to the same curve.

③ Output is disabled (open circuit), $\overline{CE}$ is at logic 1.

④ All device pins at 0 volts except pin under test at $0 \leq V_{IN} \leq 5.5$ volts.

⑤ $0V \leq V_{OUT} \leq +5.5V$.

⑥ During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished

⑦ Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.

AC CHARACTERISTICS ② ⑦

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$ ①

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		4104-30		4104-32		4104-33		4104-35		4104-36			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t_C	460		310		260		230		180		ns	⑧
Random Access	t_{AC}		300		200		150		120		85	ns	③
Chip Enable Pulse Width	t_{CE}	300	10,000	200	10,000	150	10,000	120	10,000	85	10,000	ns	
Chip Enable Precharge Time	t_P	150		100		100		100		85		ns	
Address Hold Time	t_{AH}	165		110		95		75		60		ns	
Address Set-Up Time	t_{AS}	0		0		0		0		0		ns	
Output Buffer Turn-Off Delay	t_{OFF}	0	75	0	50							ns	⑨
Read Command Set-Up Time	t_{RS}	0		0		0		0		0		ns	④
Write Enable Set-Up Time	t_{WS}	−20		−20		0		0		0		ns	④
Data Input Hold Time Referenced to $\overline{WE}$	t_{DIH}	25		25		20		20		20		ns	
Write Enabled Pulse Width	t_{WW}	90		60		55		50		45		ns	
Modify Time	t_{MOD}	0	10,000	0	10,000	0	10,000	0	10,000	0	10,000	ns	⑤
WE to CE Precharge Lead Time	t_{WPL}	105		70		65		60		55		ns	⑥
Data Input Set-Up Time	t_{DS}	0		0		0		0		0		ns	
Write Enable Hold Time	t_{WH}	225		150		115		90		65		ns	
Transition Time	t_T	5	50	5	50	5	50	5	50	5	50	ns	
Read-Modify-Write Cycle Time	t_{RMW}	565		380		325		290		235		ns	⑩

Notes:
① All voltages referenced to V_{SS}.
② During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.
③ Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.
④ If $\overline{WE}$ follows $\overline{CE}$ by more than t_{WS} then data out may not remain open circuited.
⑤ Determined by user. Total cycle time cannot exceed t_{CE} max.
⑥ Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.
⑦ AC measurements assume $t_T = 5$ ns. Timing points are taken as $V_{IL} = 0.8V$ and $V_{IH} = 2.2V$ on the inputs and $V_{OL} = 0.4V$ and $V_{OH} = 2.4V$ on the output waveform.
⑧ $t_C = t_{CE} + t_P + 2\,t_T$.
⑨ The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
⑩ $t_{RMW} = t_{AC} + t_{WPL} + t_P + 3\,t_T + t_{MOD}$.

STANDBY CHARACTERISTICS

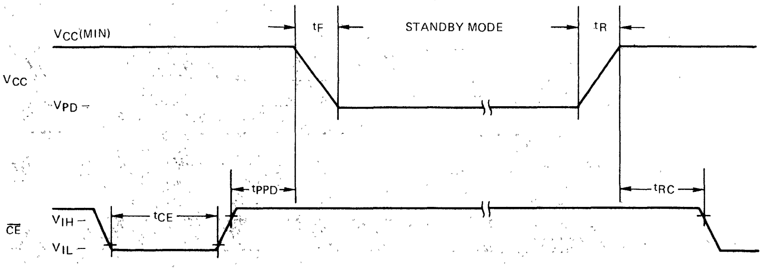
$T_a = 0°C$ to $+70°C$

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		4104 30		4104-32		4104-33		4104-35		4104-36			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V_{CC} In Standby	V_{PD}	3.0		3.0		3.0		3.0		3.0		V	
Standby Current	I_{PD}		3.3		3.3		3.3		3.3		3.3	mA	①
Power Supply Fall Time	T_F	100		100		100		100		100		μs	
Power Supply Rise Time	T_R	100		100		100		100		100		μs	
Chip Enable Pulse $\overline{CE}$ Width	T_{CE}	300		200		150		120		85		μs	
Chip Enable Precharge To Power Down Time	T_{PPD}	150		100		100		100		85		ns	
"I" Level $\overline{CE}$ Min Level	V_{IH}	2.2		2.2		2.2		2.2		2.2		V	
Standby Recovery Time	T_{RC}	500		500		500		500		500		μs	

Note ① Maximum value for I_{PD} is guaranteed at V_{PD} minimum value (=3V).

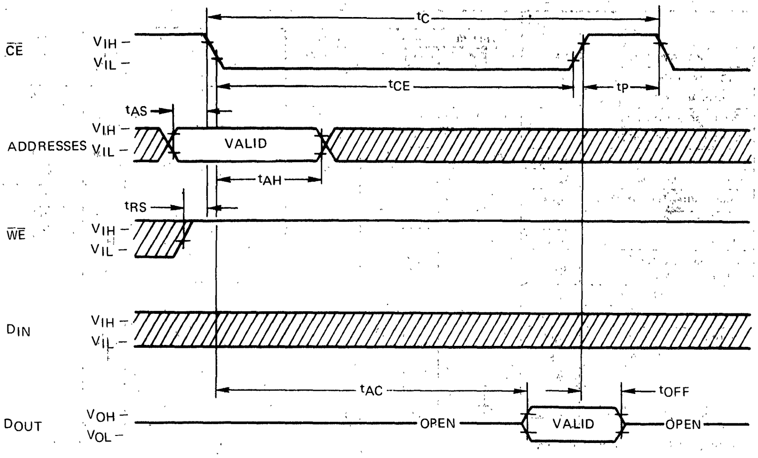
TIMING WAVEFORMS

POWER DOWN

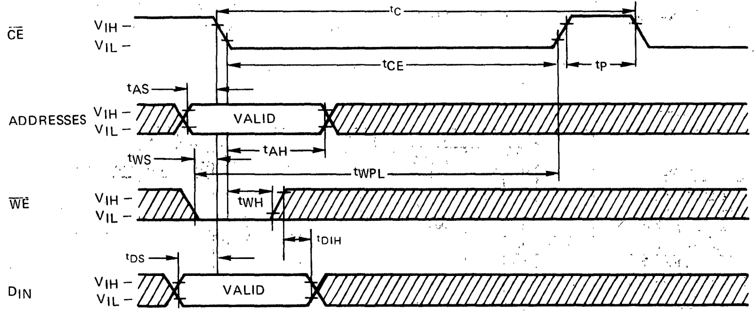


TIMING WAVEFORMS (CONT.)

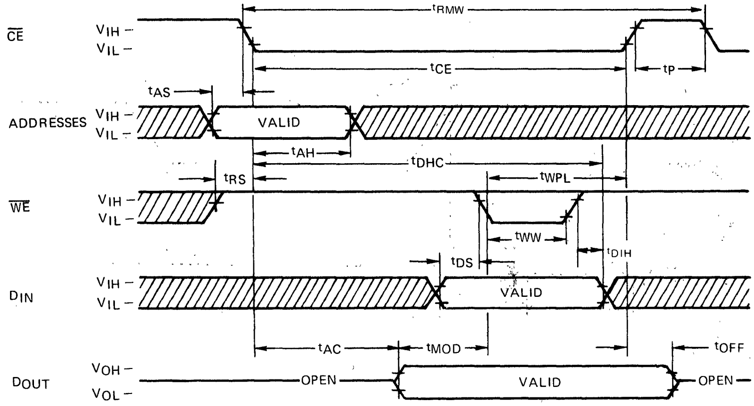
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



OPERATIONAL DESCRIPTION

READ CYCLE

The selection of one of the possible 4096 bits is made by virtue of the 12 address bits presented at the inputs. These are latched into the chip by the negative going edge of chip enable ($\overline{CE}$). If the write enable ($\overline{WE}$) input is held at a high level (V_{IH}) while the $\overline{CE}$ input is clocked to a low level (V_{IL}), a read operation will be performed. At the access time (t_{AC}), valid data will appear at the output. Since the output is unlatched by a positive transition of $\overline{CE}$, it will be in the high impedance state from the previous cycle until the access time. It will go to the high impedance state again at the end of the current cycle when $\overline{CE}$ goes high.

The address lines may be set up for the next cycle any time after the address hold time has been satisfied for the current cycle.

WRITE CYCLE

Data to be written into a selected cell is latched into the chip by the later negative transition of $\overline{CE}$ or $\overline{WE}$. If $\overline{WE}$ is brought low before $\overline{CE}$, the cycle is an "Early Write" cycle, and data will be latched by $\overline{CE}$. If $\overline{CE}$ is brought low before $\overline{WE}$, as in a Read-Modify-Write cycle, then data will be latched by $\overline{WE}$.

If the cycle is an "Early Write" cycle, the output will remain in the high impedance state. For a Read-Modify-Write cycle; the output will be active for the Modify and Write portions of the memory cycle until $\overline{CE}$ goes high. If $\overline{WE}$ is brought low after $\overline{CE}$ but before the access time, the state of the output will be undefined. The desired data will be written into the cell if data-in is valid on the leading edge of $\overline{WE}$, t_{DIH} is satisfied and $\overline{WE}$ occurs prior to $\overline{CE}$ going high by at least the minimum lead time (t_{WPL}).

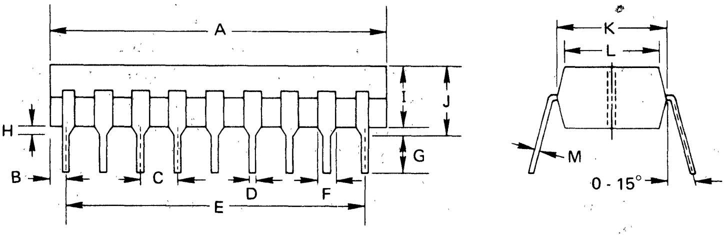
READ-MODIFY-WRITE

Read and Write cycles can be combined to allow reading of a selected location and then modifying that data within the same memory cycle. Data is read at the access time and modified during a period defined by the user. New data is written between $\overline{WE}$ low and the positive transition of $\overline{CE}$. Data out will remain valid until the rising edge of $\overline{CE}$. A minimum R-M-W cycle time can be calculated by $t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3\ t_T$; where t_{RMW} is the cycle time, t_{AC} is the access time, t_{MOD} is the user defined modify time, t_{WPL} is the $\overline{WE}$ to $\overline{CE}$ lead time, t_P is the $\overline{CE}$ high time, and t_T is one transition time.

POWER DOWN MODE

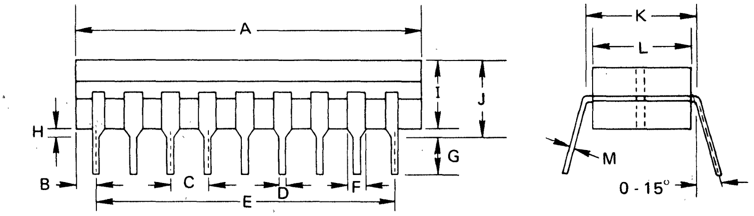
In power down, data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leqslant$4.5V) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

PACKAGE OUTLINES
µPD4104C/D



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

NEC Microcomputers, Inc.

NEC
μPD421
PRELIMINARY

8K BIT STATIC RAM

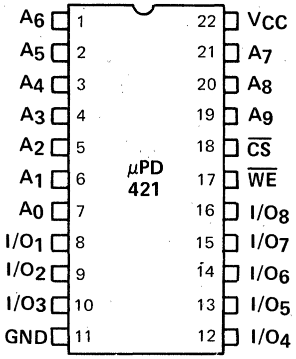
DESCRIPTION

The NEC μPD421 is a very high speed 8192 bit static Random Access Memory organized as 1024 words by 8 bits. Features include a power down mode controlled by the chip select input for an 80 percent power saving.

FEATURES

- 1024 X 8-Bit Organization
- Very Fast Access Time: 85/100/150/200 ns
- Single +5V Power Supply
- Low Power Standby Mode
- N-Channel Silicon Gate Process
- Fully TTL Compatible
- Six-Device Static Cell
- Three State Common I/O
- Compatible with 8108 and Equivalent Devices
- Available in a 22-Pin Dual-in-Line Package

PIN CONFIGURATION



NEC Microcomputers, Inc.

NEC

μPD443/6508
μPD443/6508-1
PRELIMINARY

1024 BIT CMOS RANDOM ACCESS MEMORY

DESCRIPTION

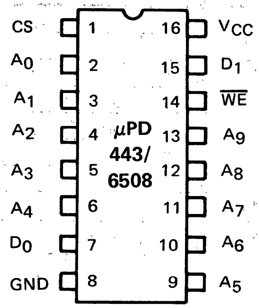
The μPD443/6508 is a high speed, low power, silicon gate CMOS 1024 bit static RAM organized as 1024 words by 1 bit. In all static states this RAM exhibits the microwatt power requirements typical of CMOS.

Inputs and three state output are TTL compatible. The basic part operates at 4 to 7 volts with a +5V, 25°C access time of 200 ns and supply current of 100 μA. Data retention is guaranteed to 3V on all parts.

FEATURES

- Low Power Operation
- Excellent Speed Operation
- TTL Compatible on Inputs and Outputs
- Static Operation
- On-Chip Address Register
- Replacement for IM 6508 and Equivalent Devices
- Available in Standard 16 Pin Ceramic Package

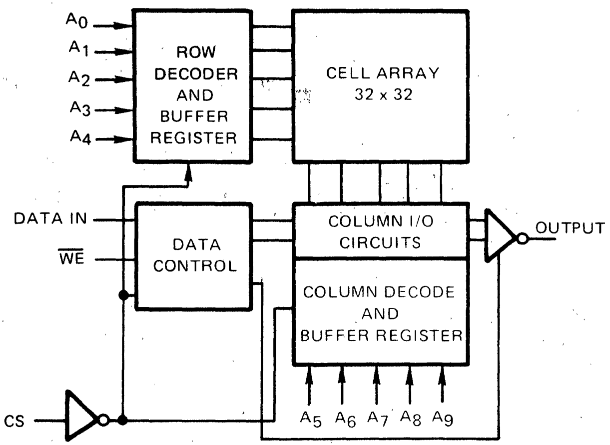
PIN CONFIGURATION



PIN NAMES

A_0-A_9	Address Input
CS	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
D_I	Data Input
D_O	Data Output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Input Voltages	−0.5 to V_{CC} +0.5 Volts
Output Voltages	−0.5 to V_{CC} +0.5 Volts
Supply Voltage	+8 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Logical "1" Input Voltage	V_{IH}	V_{CC}−2.0			V	
Logical "0" Input Voltage	V_{IL}			0.8	V	
Input Leakage	I_{IL}	−1.0		1.0	μA	0V ≤ V_{IN} ≤ V_{CC}
Logical "1" Output Voltage	V_{OH2}	V_{CC}−0.01			V	I_{OUT} = 0
Logical "1" Output Voltage	V_{OH1}	2.4			V	I_{OH} = −0.2 mA
Logical "0" Output Voltage	V_{OL2}			GND+0.01	V	I_{OUT} = 0
Logical "0" Output Voltage	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
Output Leakage	I_O	−1.0		1.0	μA	0V ≤ V_O ≤ V_{CC}
Supply Current	I_{CC}		1.0	100	μA	V_{IN} = V_{CC}

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5.0	7.0	pF	
Output Capacitance	C_{OUT}		6.0	10.0	pF	

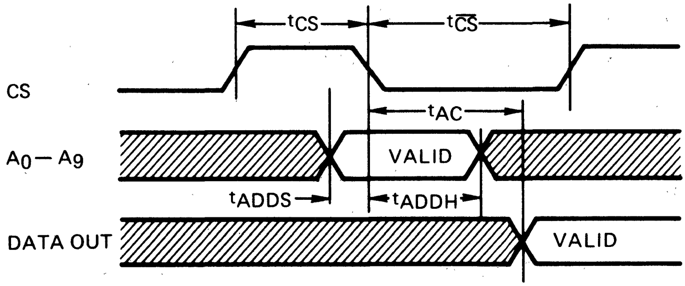
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		μPD443/6508-1		μPD443/6508			
		MIN	MAX	MIN	MAX		
Access Time From CS	t_{AC}		250		300	ns	$t_r = t_f = 20$ ns $V_{ref} = 50\%$ Load = 1 TTL Gate $C_L = 50$ pF
Output Enable Time	t_{EN}		180		180	ns	
Output Disable Time	t_{DIS}		180		180	ns	
CS Pulse Width (Positive)	t_{CS}	150		165		ns	
CS Pulse Width (Negative)	$t_{\overline{CS}}$	250		300		ns	
Write Pulse Width (Negative)	t_{WP}	165		165		ns	
Address Set Up Time	t_{ADDS}	7		7		ns	
Address Hold Time	t_{ADDH}	90		90		ns	
Data Set Up Time	t_{DS}	165		165		ns	
Data Hold time	t_{DH}	0		0		ns	

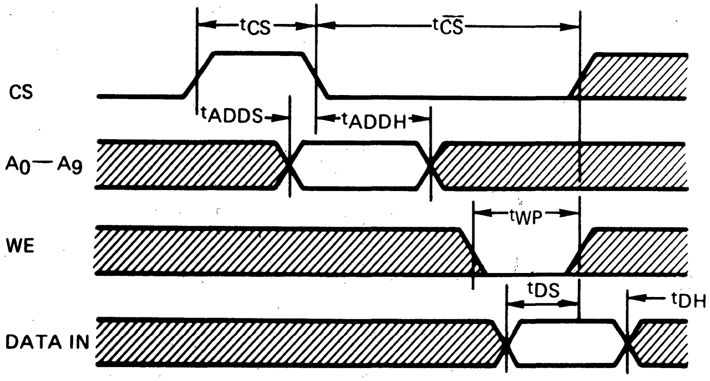
TIMING WAVEFORMS

READ CYCLE



Note: ① The μPD443/6508 output is active when CS is low.

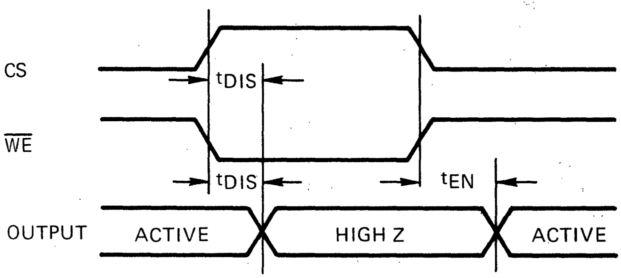
WRITE CYCLE



Notes: ① The μPD443/6508 performs a write operation when CS = WE = 0.
② The write operation is terminated on the positive edge from CS.

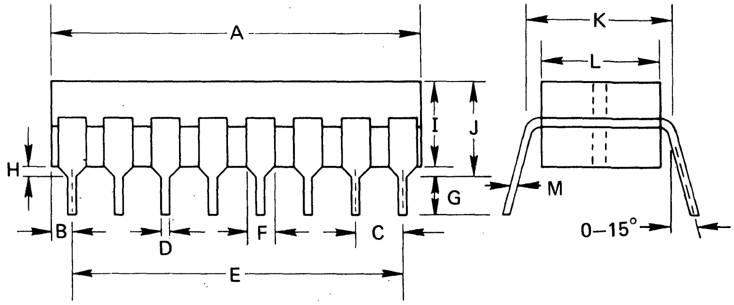
TIMING WAVEFORMS (CONT.)

OUTPUT ENABLE



Note: ① μPD443/6508 output is high impedance when CS = 1 or $\overline{WE}$ = 0.

PACKAGE OUTLINE μPD443/6508D



ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

NEC Microcomputers, Inc.

NEC
μPD5101L
μPD5101L-1

1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the devices being selected when $\overline{CE}_1$ is low and CE_2 is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

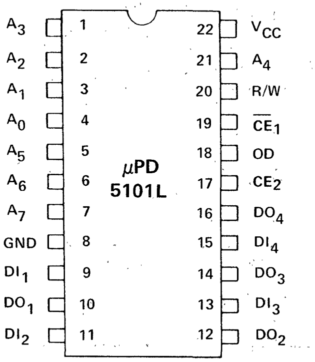
The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 650 ns (μPD5101L); 450 ns (μPD5101L-1)
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode
- Available in a 22-pin Dual-in-Line Package

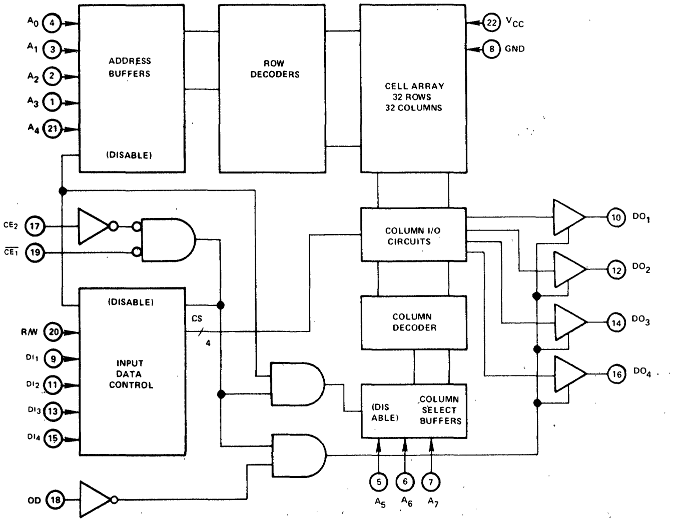
PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . 0°C to +70°C
Storage Temperature . . . . −40°C to +125°C
Voltage On Any Pin With Respect to Ground . . . . −0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage . . . . −0.3 to +7.0 Volts

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP ①	MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} ②			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} ②			−1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} ②			1	μA	$\overline{CE}_1$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} ②			−1	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}			22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Operating Current	I_{CC2}			27	mA	V_{IN} = 2.2V Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Standby Current	I_{CCL} ②			10	μA	V_{IN} = 0 to 5.25V CE_2 ≤ 0.2V
Input Low Voltage	V_{IL}	−0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = −100 μA

Notes: ① Typical values at T_a = 25°C and nominal supply voltage.
② Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} 0V

AC CHARACTERISTICS

READ CYCLE

$T_a = 0°C$ to $70°C$; $V_{CC} = 5V±5\%$, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Read Cycle	t_{RC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts Input rise and fall times: 20 ns Timing measurement reference level: 1.5 Volt Output load: I_{TTL} Gate and C_L = 100 pF
Access Time	t_A			650			450	ns	
Chip Enable ($\overline{CE}_1$) to Output	t_{CO1}			600			400	ns	
Chip Enable (CE_2) to Output	t_{CO2}			700			500	ns	
Output Disable to Output	t_{OD}			350			250	ns	
Data Output to High Z State	t_{DF}	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0			0			ns	

WRITE CYCLE

$T_a = 0°C$ to $70°C$; $V_{CC} = 5V±5\%$, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Write Cycle	t_{WC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts Input rise and fall times: 20 ns Timing measurement reference level: 1.5 Volt Output load: I_{TTL} Gate and C_L = 100 pF
Write Delay	t_{AW}	150			130			ns	
Chip Enable ($\overline{CE}_1$) to Write	t_{CW1}	550			350			ns	
Chip Enable (CE_2) to Write	t_{CW2}	550			350			ns	
Data Setup	t_{DW}	400			250			ns	
Data Hold	t_{DH}	100			50			ns	
Write Pulse	t_{WP}	400			250			ns	
Write Recovery	t_{WR}	50			50			ns	
Output Disable Setup	t_{DS}	150			130				

LOW V_{CC} DATA RETENTION CHARACTERISTICS

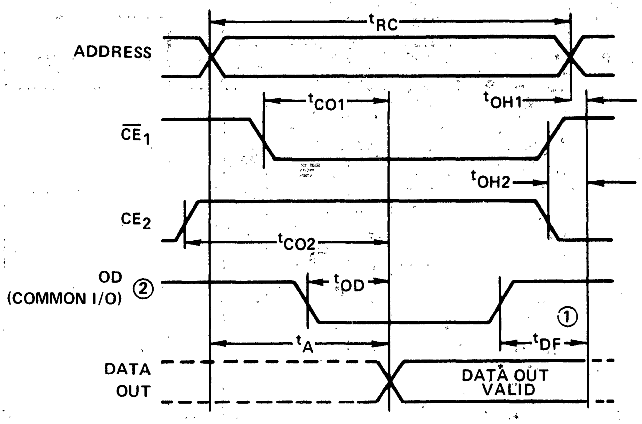
$T_a = 0°C$ to $70°C$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leqslant +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	$V_{CCDR} = +2.0V$ $CE_2 \leqslant +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC}①			ns	

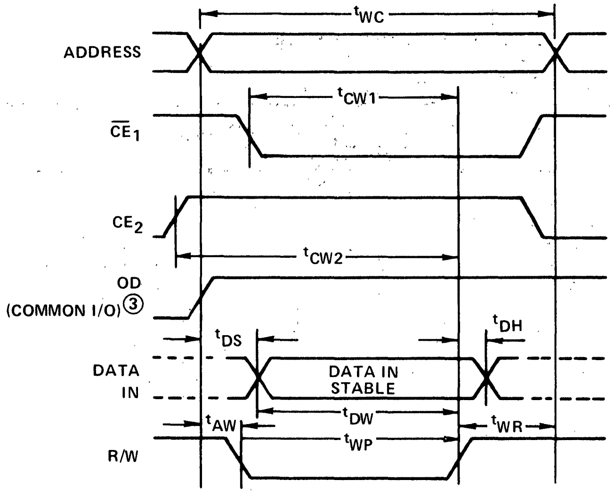
Note: ① t_{RC} = Read Cycle Time

TIMING WAVEFORMS

READ CYCLE

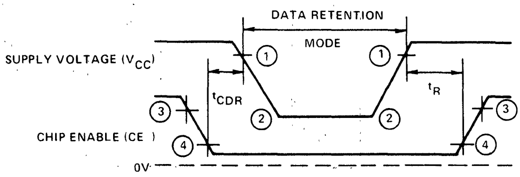


WRITE CYCLE



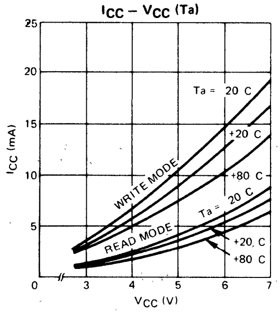
Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

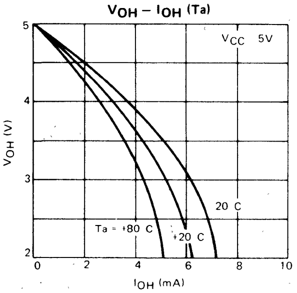
LOW V_{CC} DATA RETENTION

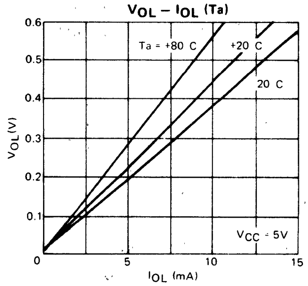


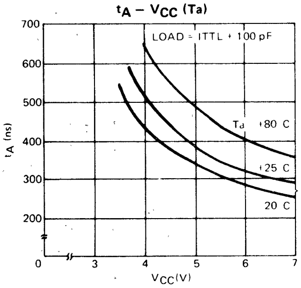
Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

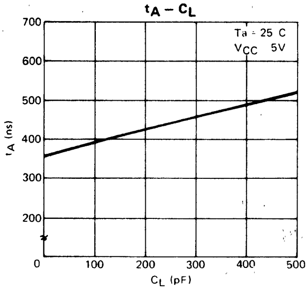
TYPICAL OPERATING CHARACTERISTICS

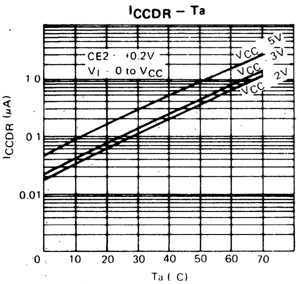

$I_{CC} - V_{CC}$ (Ta)


$V_{OH} - I_{OH}$ (Ta)

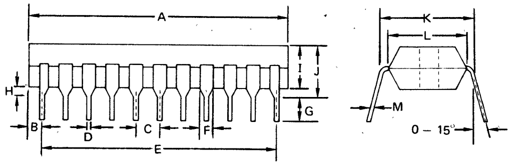

$V_{OL} - I_{OL}$ (Ta)


$t_A - V_{CC}$ (Ta)


$t_A - C_L$


I_{CCDR} – Ta

PACKAGE OUTLINE μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 ± 0.10	0.02 ± 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

NEC Microcomputers, Inc.

NEC

μPD444/6514

PRELIMINARY

1K X 4 BIT STATIC CMOS RAM

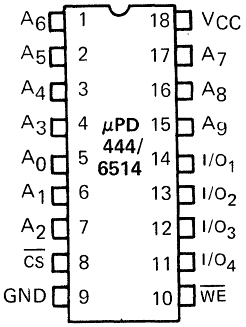
DESCRIPTION

The NEC μPD444/6514 is a 4096 bit Random Access Memory fabricated using the NEC CMOS process. This yields devices with low operating power and standby currents of exceptionally low magnitude. These characteristics make the μPD444/6514 ideal for applications requiring battery backup. In addition, the compatibility of the μPD444/6514 with 2114-type devices affords the designer a higher degree of flexibility.

FEATURES

- Low Power Operation
- Excellent Speed Operation (300 ns access time)
- TTL Compatible on Inputs and Outputs
- Completely Static Operation
- Single +5V Supply
- Common Data Input and Output Using Three-State Outputs
- The Basic Part Operates at +4V to +7V
- Data Retention is Guaranteed to +2V on All Parts
- Replacement for 2114 and Equivalent Devices

PIN CONFIGURATION



NEC

μPD445L
μPD445L-1

FULLY DECODED 4096 STATIC CMOS RAM

DESCRIPTION

The μPD445L is a very low power 4,096 bit (1024 words by 4 bits) static RAM fabricate with NEC's complementary MOS (CMOS) process. It has two chip enable inputs ($\overline{CE}_1$, CE_2). Minimum standby current is drawn when $\overline{CE}_1$ is at a high level, while inhibiting all address and control line transitions or, unconditionally when CE_2 is at a low level. This device ideally meets the low power requirements of battery operated systems and battery back-up systems for non-volatility of data.

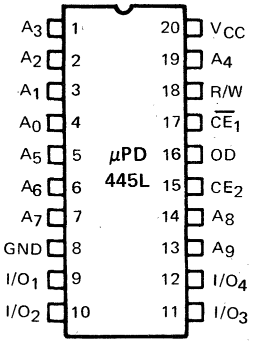
The μPD445L uses fully static circuitry requiring no clocking. Output data is read out non-destructively by placing a high on the R/W pin and has the same polarity as input data. All inputs and outputs are directly TTL compatible. The device has common input/output data busses and an OD (Output Disable) pin for use in common I/O bus systems.

The μPD445L is guaranteed to retain data with the power supply voltage as low as 2.0 volts.

FEATURES

- Single +5V Power Supply
- Ideal for Battery Operation
- Low Standby Power for Data Retention
- Simple Memory Expansion — Chip Enable Inputs
- Access Time — 650 ns Max. (μPD445L)
  450 ns Max. (μPD445L-1)
- Directly TTL Compatible — All Inputs and Outputs
- Common Data Input and Output
- Static CMOS — No Clocks Refreshing Required
- 20 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



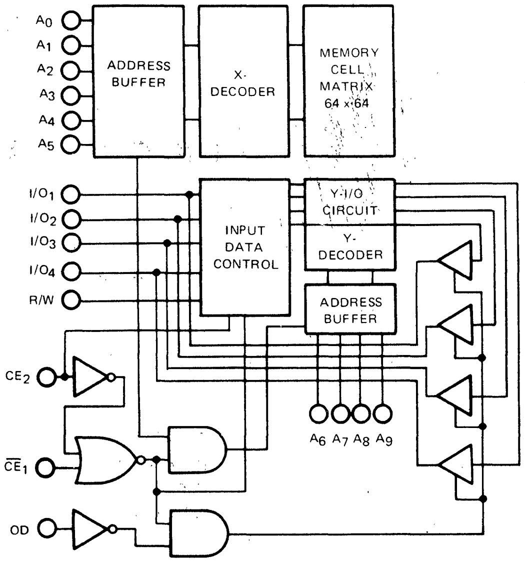
PIN NAMES

A_0-A_9	Address Input
OD	Output Disable
R/W	Read/Write
$\overline{CE}_1$	Chip Enable 1
CE_2	Chip Enable 2
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power Supply
GND	Ground

OPERATION MODES

$\overline{CE}_1$	CE_2	OD	Chip	Output Mode
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			Non-Selected	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to $+70^\circ$C
Storage Temperature	-40°C to $+125^\circ$C
All Output Voltages	-0.3 to V_{CC} $+0.3$ Volts
All Input Voltages	-0.3 to V_{CC} $+0.3$ Volts
Supply Voltage V_{CC}	-0.3 to $+7$ Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25^\circ$C

DC CHARACTERISTICS

$T_a = -10$ to $+70^\circ$C; $+5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3		+ 0.65	V	
Output High Voltage	V_{OH1}	+2.4			V	$I_{OH} = -1.0$ mA
	V_{OH2}	+3.5			V	$I_{OH} = -100$ µA
Output Low Voltage	V_{OL}			+ 0.4	V	$I_{OL} = +2.0$ mA
Input Leakage Current High	I_{LIH}			+ 1.0	µA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			− 1.0	µA	$V_I = 0V$
Output Leakage Current High	I_{LOH}			+ 1.0	µA	$V_O = V_{CC}$, $\overline{CE}_1 = 2.2V$
Output Leakage Current Low	I_{LOL}			− 1.0	µA	$V_O = 0V$, $\overline{CE}_1 = 2.2V$
Supply Current	I_{CC1}		12	25	mA	Outputs Open $V_I = V_{CC}$ except $\overline{CE}_1 \leqslant 0.65V$
Supply Current	I_{CC2}		16	30	mA	Outputs Open $V_I = 2.2V$ except $\overline{CE}_1 \leqslant 0.65V$
Standby Current	I_{CCL}			40	µA	$V_I = 0$ to $5.25V$ Except $CE_2 \leqslant 0.2V$

AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		445L		445L-1			
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	650		450		ns	
Access Time	t_A		650		450	ns	Input Voltage Levels
Chip Enable $(\overline{CE}_1)$ to Output	t_{CO1}		600		400	ns	V = +0.65 to +2.2V
Chip Enable (CE_2) to Output	t_{CO2}		700		500	ns	Input Rise Time 20 ns
Output Enable to Output	t_{OD}		350		250	ns	Input Fall Time 20 ns
Output Disable (OD) to Floating	t_{DF}	0	150	0	130	ns	Timing Measurement Reference Level = +1.5V
Data Output Hold Time	t_{OH1}	0		0		ns	Output Load
Chip Disable to Floating	t_{OH2}	0		0		ns	1 TTL + 100 pF
Address Rise and Fall Time	t_r t_f		300		300	ns	For Address change during Chip Enabled

WRITE CYCLE

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		445L		445L-1			
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	650		450		ns	
Address Setup Time	t_{AW}	150		130		ns	Input Voltage Levels $V_I = +0.65$ to $+2.2V$
Chip Enable $(\overline{CE}_1)$ to Write End	t_{CW1}	550		350		ns	Input Rise Time 20 ns
Chip Enable (CE_2) to Write End	t_{CW2}	550		350		ns	Input Fall Time 20 ns
Data Setup Time	t_{DW}	400		250		ns	
Data Hold Time	t_{DH}	100		50		ns	Timing Measurement
Write Pulse Width	t_{WP}	400		250		ns	Reference Level = +1.5V
Address Hold Time	t_{WR}	50		50		ns	
Output Disable Setup Time	t_{DS}	150		130		ns	
Address Rise and Fall Time	t_r t_f		300		300	ns	For Address change during Chip Enabled

LOW V_{CC} DATA RETENTION

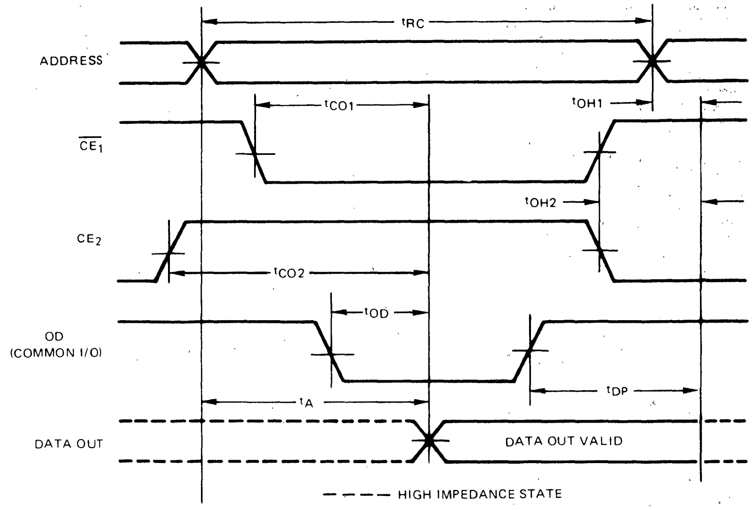
$T_a = -10°C$ to $+70°C$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leqslant +0.2V$
Data Retention Current	I_{CCDR}			40	μA	$V_{CCDR} = +2.0V$ $CE_2 \leqslant +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC} ①			ns	

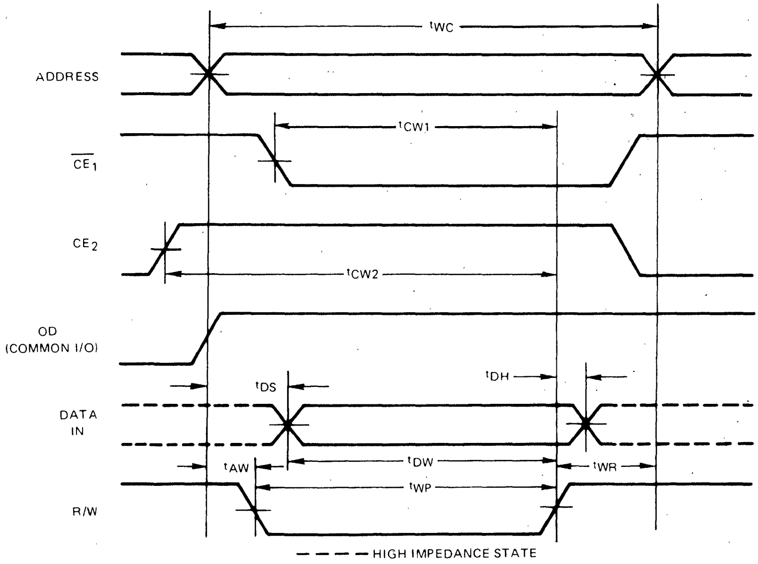
Note: ① t_{RC} = Read Cycle Time

TIMING WAVEFORMS

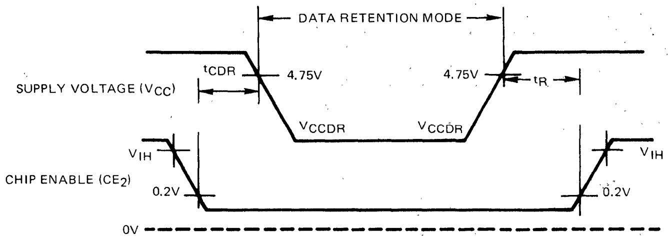
READ CYCLE



WRITE CYCLE



LOW V_{CC} DATA RETENTION ①



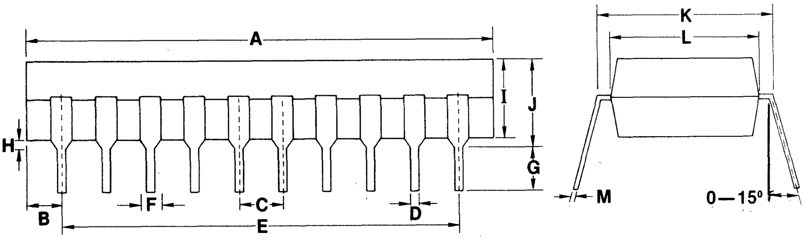
Note ① Apply less than V_{CCDR} to all inputs for data retention mode.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I		5	8	pF	$V_I = 0V$
Output Capacitance	C_O		8	12	pF	$V_O = 0V$

PACKAGE OUTLINE µPD445LC



ITEM	MILLIMETERS	INCHES
A	27.00	1.07
B	2.07	0.08
C	2.54	0.10
D	0.50	0.02
E	22.86	0.90
F	1.20	0.05
G	2.54 MIN	0.10 MIN
H	0.50 MIN	0.02 MIN
I	4.58 MAX	0.18
J	5.08 MAX	0.20
K	10.16	0.40
L	8.60	0.39
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

NEC Microcomputers, Inc.

NEC
μPD454

FULLY DECODED 2048 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

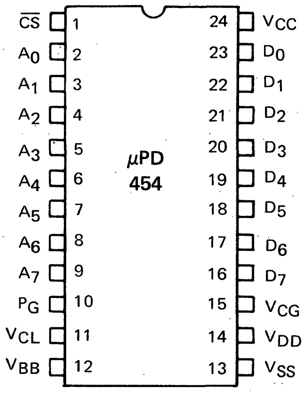
The μPD454 EEPROM, a 256 Words x 8 Bits Read Only Memory, is designed for rapid development of microcomputer systems. The ability to electrically program, erase, and reprogram the μPD454 provides a fast and convenient means of debugging both hardware and software designs.

The μPD454 is pin for pin compatible with NEC's μPD464 mask programmed ROM.

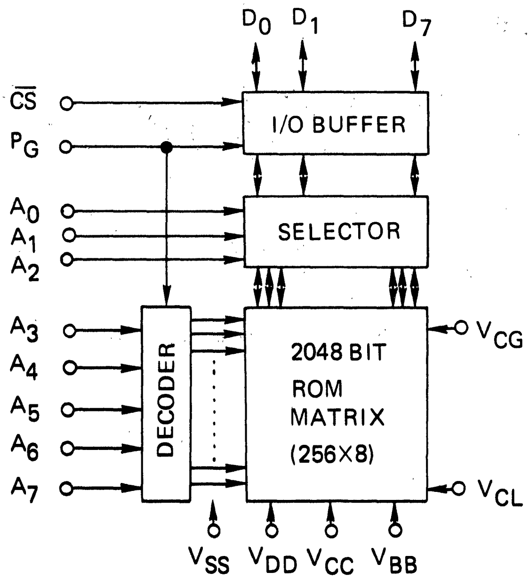
FEATURES

- Electrically Erasable and Programmable
- Fully Decoded, 256 Words x 8 Bits Organization
- Access Time 800 ns Max
- Low Power: 245 mW (Typ.) in Read Operation
  670 mW (Typ.) in Programming Operation
- Fast Programming and Erasure Speed
- Low Power for Programming and Erasure
- Static, No Clock Required
- Input/Output TTL Compatible for Read and Programming Operation
- Three-State Output, OR-Tie Capability
- N-Channel MOS Fabrication
- Two Power Supplies, +12V and +5V for Read Operation
- 24 Pin Ceramic DIP

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . −10°C to +70°C
Storage Temperature . . . . −40°C to +125°C
All Output Voltages . . . . −0.3 to +11 Volts①
All Input Voltages . . . . −0.3 to +11 Volts ①
Supply Voltage V_{DD} . . . . −0.3 to +15 Volts①
Supply Voltage V_{CC} . . . . −0.3 to +7 Volts ①
Supply Voltage V_{BB} . . . . V_{SS} to −7 Volts②
Supply Voltage P_G . . . . −0.3 to +30 Volts① ②
Supply Voltage V_{CL} . . . . −0.3 to +43 Volts① ②
Supply Voltage V_{CG} . . . . −44 to +30 Volts① ②

Notes: ① Relative to V_{BB}.
② Data in the memory cell is not guaranteed to be preserved.
Specifies ratings which will not cause permanent damage to the device.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$^*T_a = 25°C$

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	f = 1 MHz

PIN DEFINITION

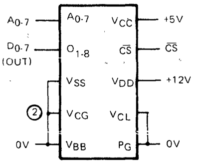
PIN			FUNCTION
NO.	SYMBOL	NAME	
1	$\overline{CS}$	CHIP SELECT	Chip selection, active low
2-9	A_0–A_7	ADDRESS BUS	Memory address
10	P_G	+26V (TYP) Power Supply	Power supply for programming operation
11	V_{CL}	+36V (TYP) Power Supply	Power supply for erasing operations
12	V_{BB}	Substrate Power Supply	Power supply
13	V_{SS}	GROUND	Ground Reference
14	V_{DD}	+12V Power Supply	Power supply for read operations
15	V_{CG}	−44 to +30 Power Supply	Power supply for control of programming and erasure operations
16-23	D_7–D_0	Data Input/Output	Data In for programming operations. Data Output for read operations.
24	V_{CC}	+5V Power Supply	Power supply for read operations

SUPPLY VOLTAGES

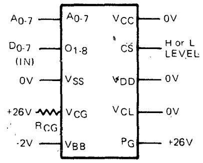
Typical values. Unit - Voltage.

MODE \ PIN	V_{DD}(14)	V_{CC}(24)	V_{BB}(14)	P_G(10)	V_{CL}(11)	V_{CG}(15)	V_{SS}(13)
Read	+12	+5	0	0	0	0	0
Program	0	0	2	+26	0	+26	0
Erase	0	0	-5	0	+36	40	Open
Verify "0"	+12	+5		0	0	+3	0
Verify "1"	+12	+5		0	0	-3	0

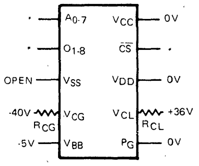
READ



PROGRAM



ERASE

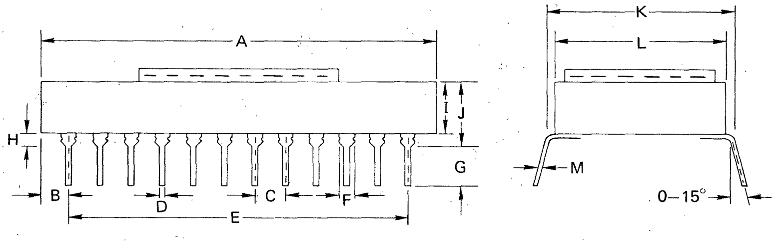


Notes: * = Either High or Low Level, or Open.

① R_{CG} and R_{CL} are Protection Resistors
R_{CG} = 10 kΩ ± 10%, 1/4W
R_{CL} = 200Ω ± 10%, 10W

② R_{CG} may be left connected in Read Mode

PACKAGE OUTLINE
μPD454D



ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

READ OPERATION

DC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

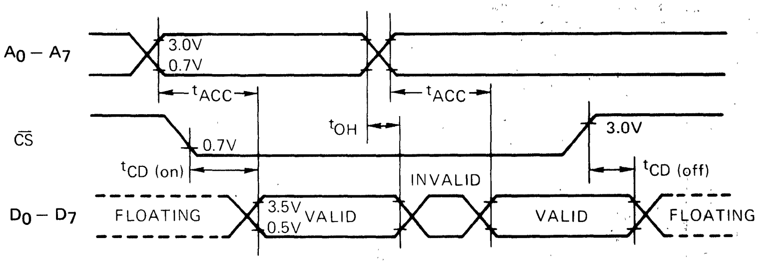
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Output High Voltage	V_{OH}	3.5			V	$I_{OH} = -2.0$ mA
Output Low Voltage	V_{OL}			0.5	V	$I_{OL} = 1.7$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = +3.0V$
Input Leakage Current Low	I_{LIL}			-10	μA	$V_I = +0.7V$
Output Leakage Current High	I_{LOH}			**+100**	μA	$\overline{CS}$ = "1" $V_O = 3.5V$
Output Leakage Current Low	I_{LOL}			-10	μA	$\overline{CS}$ = "1" $V_O = 0.4V$
V_{DD} Supply Current	I_{DD}		**20**		mA	
V_{CC} Supply Current	I_{CC}			**0.3**	mA	with no load

AC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Access Time	t_{ACC}			**800**	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	$t_{CD(on)}$			200	ns	
$\overline{CS}$ to Output Off Delay	$t_{CD(off)}$	0		200	ns	
Output Hold Time	t_{OH}	0			ns	

TIMING WAVEFORMS



PROGRAMMING OPERATION

Before the μPD454 is programmed the device must be erased. All bit locations must contain a zero (0). The μPD454 programming procedure is word by word one word at a time.

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

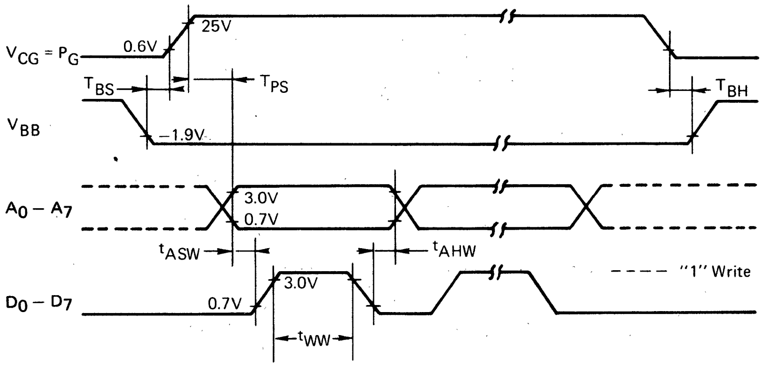
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Supply Voltage	V_{BB}	−1.9	−2.0	−2.1	V	
Supply Voltage	P_G	25	26	27	V	
Supply Voltage	V_{CG}	25	26	27	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}		−8		mA	
Supply Current (P_G)	I_G		+25		mA	
Supply Current (V_{CG})	I_{CG}			+10	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Setup Time	t_{ASW}	10			μs	
Address Hold Time	t_{AHW}	10			μs	
Write Data Width	t_{WW}	20		100	ms	per one word
V_{BB} Setup Time	T_{BS}	1.0			μs	
V_{BB} Hold Time	T_{BH}	1.0			μs	
P_G, V_{CG} Setup Time	T_{PS}	10			μs	

TIMING WAVEFORMS



ERASURE OPERATION*

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$
$\overline{CS}$, $A_0 - A_7$ and $D_0 - D_7$ = Either HIGH or LOW level, or non-connected

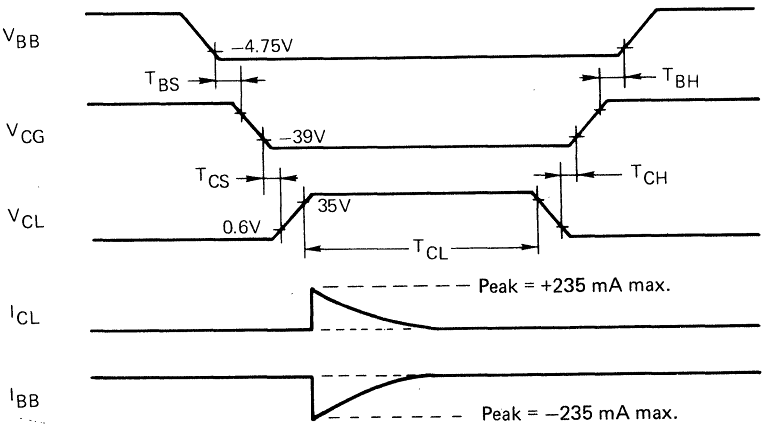
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{BB}	−4.75	−5.0	−5.25	V	
Supply Voltage	V_{CL}	+35	+36	+37	V	through R_{CL}
Supply Voltage	V_{CG}	−39	−40	−41	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}			−235	mA	Initial peak current. See timing chart.
Supply Current (V_{CL})	I_{CL}			−235	mA	
Supply Current (V_{CG})	I_{CG}			−20	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$
$\overline{CS}$, $A_0 - A_7$ and $D_0 - D_7$ = Either HIGH or LOW level, or non-connected

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clear Time	T_{CL}			60	sec	
V_{BB} Setup Time	T_{BS}	0			μs	
V_{BB} Hold Time	T_{BH}	0			μs	
V_{CG} Setup Time	T_{CS}	1.0			μs	
V_{CG} Hold Time	T_{CH}	1.0			μs	

TIMING WAVEFORMS



Note: The supply currents I_{BB} and I_{CL} diminish to almost zero within T_{CL}

*Erasure operation clears all 2048 bits to Logic "0" simultaneously.

NEC Microcomputers, Inc.

NEC
μPD458

FULLY DECODED 8192 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

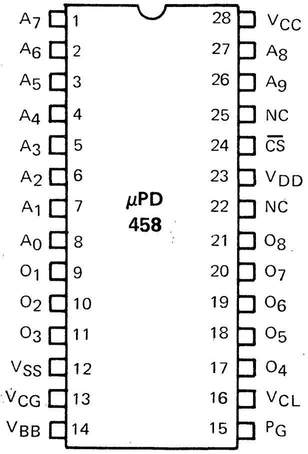
The μPD458 is an Electrically Erasable and Reprogrammable Read Only Memory (EEPROM), organized as 1024 words by 8 bits.

The μPD458 is fabricated with N-channel MOS technology and is packaged in a 28 pin ceramic DIP.

FEATURES

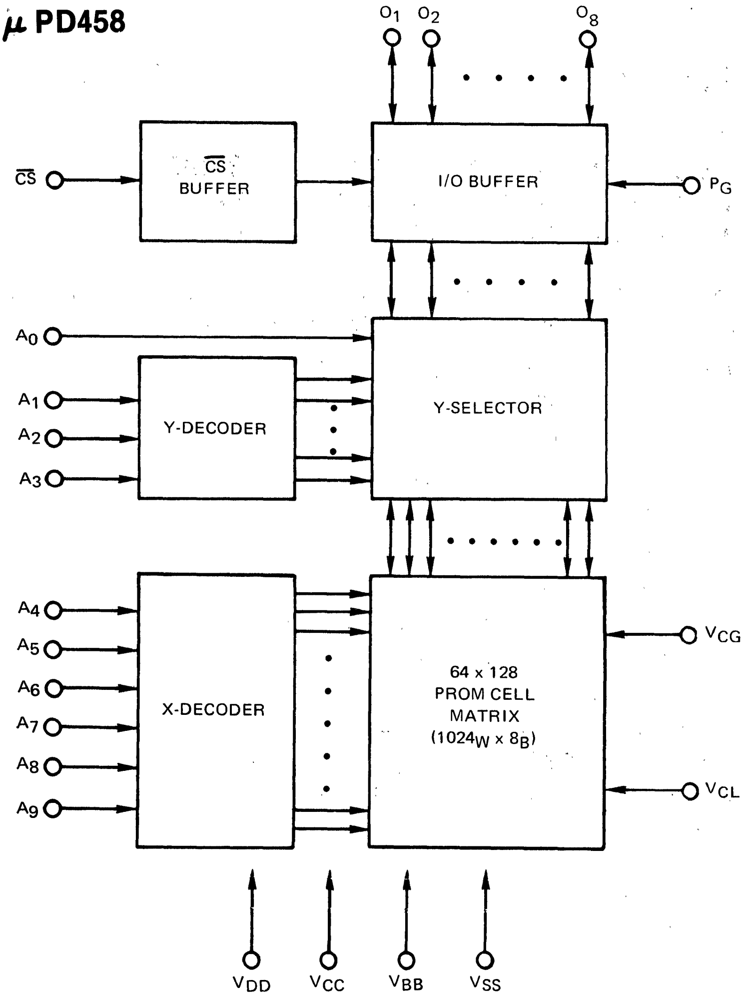
- Electrically Erasable and Reprogrammable
- Fully Decoded, 1024 Words x 8 Bits Organization
- Access Time – 450 ns max.
- Fast Programming and Erasure Speed
- Simple Worst-case Verification of Programmed Data and Erasure
- Static, No Clock Required
- Input/Output TTL Compatible for Read and Programming Operation
- Three-State Output, OR-Tie Capability
- N-Channel MOS
- Two Power Supplies, +12V and +5V for Read
- 28 Pin Ceramic DIP

PIN CONFIGURATION



NC: No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.3 to +11 Volts①
All Input Voltages	−0.3 to +11 Volts ①
Supply Voltage V_{DD}	−0.3 to +15 Volts①
Supply Voltage V_{CC}	−0.3 to +7 Volts①
Supply Voltage V_{BB}	V_{SS} to −7 Volts②
Supply Voltage P_G	−0.3 to +30 Volts① ②
Supply Voltage V_{CL}	−0.3 to +43 Volts① ②
Supply Voltage V_{CG}	−44 to +30 Volts① ②

Notes: ① Relative to V_{BB}.
② Data in the memory cell is not guaranteed to be preserved.
Specifies ratings which will not cause permanent damage to the device.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

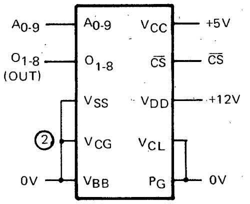
CAPACITANCE

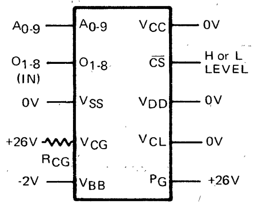
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	f = 1 MHz

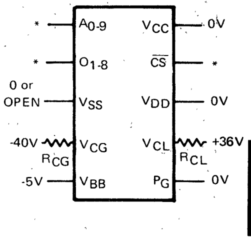
SUPPLY VOLTAGES

Typical values. Unit — Voltage.

MODE \ PIN	V_{DD}(23)	V_{CC}(28)	V_{BB}(14)	P_G(15)	V_{CL}(16)	V_{CG}(13)	V_{SS}(12)
Read	+12	+5	0	0	0	0	0
Program	0	0	−2	+26	0	+26	0
Erase	0	0	−5	0	+36	−40	0 or Open
Verify "0"	+12	+5		0	0	+3	0
Verify "1"	+12	+5		0	0		0


READ


PROGRAM


ERASE

Notes: * = Either High or Low Level, or Open.

① R_{CG} and R_{CL} are Protection Resistors
R_{CG} = 10 kΩ ± 10%, 1/4W
R_{CL} = 200Ω ± 10%, 10W

② R_{CG} may be left connected in Read Mode.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	INPUT/ OUTPUT	FUNCTION
1 – 8, 26, 27	$A_0 - A_9$	Input	Address Input
24	$\overline{CS}$	Input	Chip Select Input (Active Low)
9 – 11, 17 – 21	$O_1 - O_8$	Output	Data Out for Read Operation
		Input	Data Input for Programming Operation
15	P_G	Power Supply	Power Supply for Programming Operation
16	V_{CL}	Power Supply	Power Supply for Erasure Operation
13	V_{CG}	Power Supply	Power Supply for Control Gate for Programming and Erasure Operation
14	V_{BB}	Power Supply	Power Supply for Substrate Bias
23	V_{DD}	Power Supply	+12V Power Supply for Read Operation
28	V_{CC}	Power Supply	+5V Power Supply for Read Operation
12	V_{SS}	GND	Ground Reference

μPD458

READ OPERATION

DC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

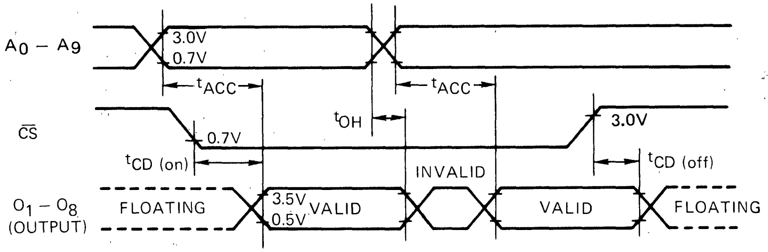
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Output High Voltage	V_{OH}	3.5			V	$I_{OH} = -2.0$ mA
Output Low Voltage	V_{OL}			0.5	V	$I_{OL} = 1.7$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = +3.0V$
Input Leakage Current Low	I_{LIL}			-10	μA	$V_I = +0.7V$
Output Leakage Current High	I_{LOH}			+20	μA	$\overline{CS}$ = "1" $V_O = 3.5V$
Output Leakage Current Low	I_{LOL}			-10	μA	$\overline{CS}$ = "1" $V_O = 0.4V$
V_{DD} Supply Current	I_{DD}		55	80	mA	
V_{CC} Supply Current	I_{CC}		20	30	mA	with no load

AC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Access Time	t_{ACC}			450	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	$t_{CD(on)}$			200	ns	
$\overline{CS}$ to Output Off Delay	$t_{CD(off)}$	0		200	ns	
Output Hold Time	t_{OH}	0			ns	

TIMING WAVEFORMS



PROGRAMMING OPERATION

Programming is performed word by word and one word at a time. Address and an 8 bit programming word for that address should be input at the same time. High level data "1" given through one of Data Input terminals ($O_1 - O_8$) writes a high level data "1" into the memory cell specified with the address input and its bit position.

After erasure, all memory cells of the μPD458 contain cleared data "0". By this programming operation, only the memory cells which contain data "0" are programmed to high level data "1" by high level input. Thus before normal programming operation, the μPD458 should undergo erasure operation to clear all bits to "0".

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

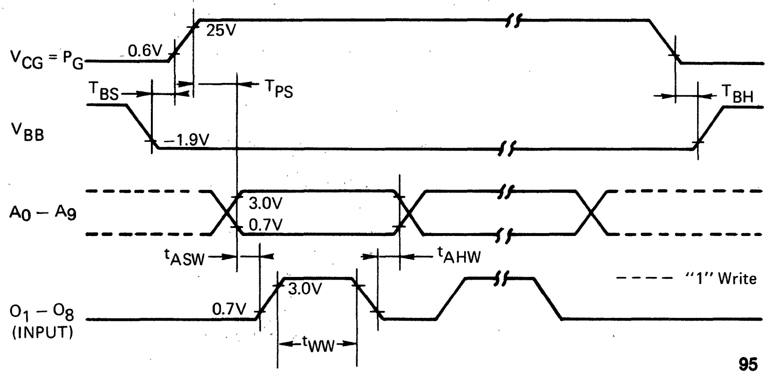
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		5.25	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Supply Voltage	V_{BB}	-1.9	-2.0	-2.1	V	
Supply Voltage	P_G	25	26	27	V	
Supply Voltage	V_{CG}	25	26	27	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}		-8	-15	mA	
Supply Current (P_G)	I_G		+30	+50	mA	
Supply Current (V_{CG})	I_{CG}			+20	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Setup Time	t_{ASW}	10			μs	
Address Hold Time	t_{AHW}	10			μs	
Write Data Width	t_{WW}	40		100	ms	per one word
V_{BB} Setup Time	T_{BS}	1.0			μs	
V_{BB} Hold Time	T_{BH}	1.0			μs	
P_G, V_{CG} Setup Time	T_{PS}	10			μs	

TIMING WAVEFORMS



ERASURE OPERATION*

DC CHARACTERISTICS

T_a = 25°C ± 2°C, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$ or Open
$\overline{CS}$, $A_0 - A_9$ and $0_1 - 0_8$ = Either HIGH or LOW level, or non-connected

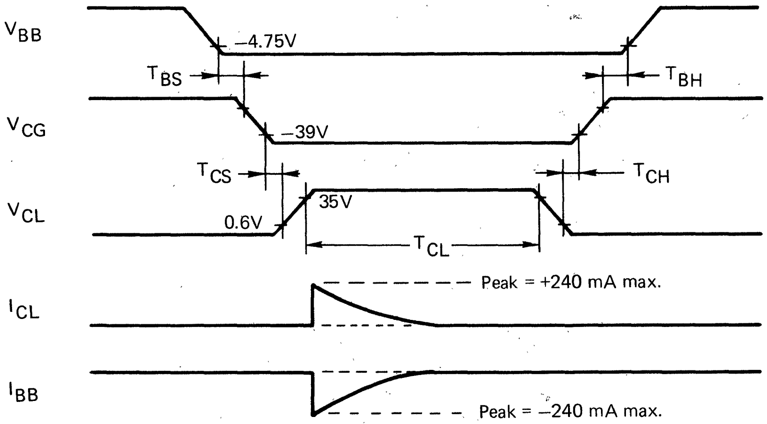
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{BB}	−4.75	−5.0	−5.25	V	
Supply Voltage	V_{CL}	+35	+36	+37	V	through R_{CL}
Supply Voltage	V_{CG}	−39	−40	−41	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}			−240	mA	Initial peak current. See timing chart.
Supply Current (V_{CL})	I_{CL}			+240	mA	
Supply Current (V_{CG})	I_{CG}			−20	μA	

AC CHARACTERISTICS

T_a = 25°C ± 2°C, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$ or Open
$\overline{CS}$, $A_0 - A_9$ and $0_1 - 0_8$ = Either HIGH or LOW level, or non-connected

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP	MAX		
Clear Time	T_{CL}		60		sec	
V_{BB} Setup Time	T_{BS}	0			μs	
V_{BB} Hold Time	T_{BH}	0			μs	
V_{CG} Setup Time	T_{CS}	1.0			μs	
V_{CG} Hold Time	T_{CH}	1.0			μs	

TIMING WAVEFORMS



Note: The supply currents I_{BB} and I_{CL} diminish to almost zero within T_{CL}.

*Erasure operation clears all 8192 bits to Logic "0" simultaneously.

APPENDIX PROM PROGRAMMER DESIGN

To insure integrity and retention of data programmed in the μPD458, the following requirements are specified for the μPD458 supply voltage and current levels. The PROM PROGRAMMER should be designed such that voltages provided to the PROM socket be within the range specified on any occasion including power on/off to the programmer, power on/off to the μPD458, and in READ, WRITE or ERASE operation. Surge or noise voltages beyond the specified range are to be avoided.

Setting V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5% and V_{CG} = +3V ± 0.1V after erasure and comparing data read from the μPD458 with zero effectively tests for proper erasure.

Setting V_{DD}= +12V ± 5%, V_{CC} = +5V ± 5% and V_{CG} = −3V ± 0.1V after programming and comparing data read from the μPD458 with the desired data coupled with erase verification, provides a simple test of worst-case temperature and long-term data retention.

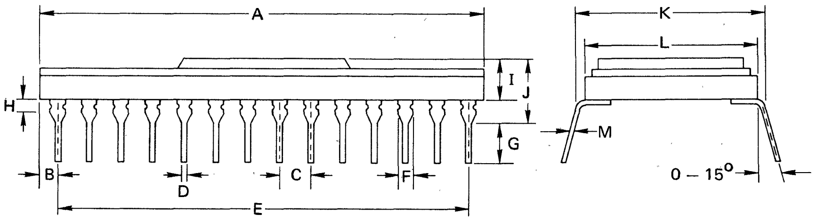
Under normal Read Mode conditions, V_{CG} should either be grounded directly or held at 0V ± 0.1V through R_{CG}. R_{CG} is required when any non-zero voltage is applied to V_{CG}.

SYMBOL	LIMITS ②									UNIT	TEST CONDITIONS
	READ			PROGRAM			ERASE				
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{DD}	+11.4	+12	+12.6	−0.3	0	+0.3	−0.3	0	+0.3	V	
V_{CC}	+4.75	+5	+5.25	−0.3	0	+0.3	−0.3	0	+0.3	V	
V_{CG}	−0.1	0	+0.1	+25	+26	+27	−39	−40	−41	V	
V_{BB}	−0.1	0	+0.1	−1.9	−2	−2.1	−4.75	−5	−5.25	V	
P_G	−0.3	0	+0.3	+25	+26	+27	−0.3	0	+0.3	V	
V_{CL}	−0.1	0	+0.1	−0.1	0	+0.1	+35	+36	+37	V	
I_{CC}		+20	+30			−0.2			−0.2	mA	①
I_{DD}		+55	+80			−0.2			−0.2	mA	①
I_{CG}			+10			+20			−20	μA	①
I_{BB}			−0.2		−8	−15			−240	mA	①
I_{PG}			−0.2		+30	+50			−0.2	mA	①
I_{CL}			−0.5			−10			+240	mA	①

Notes: ① At typical supply voltage

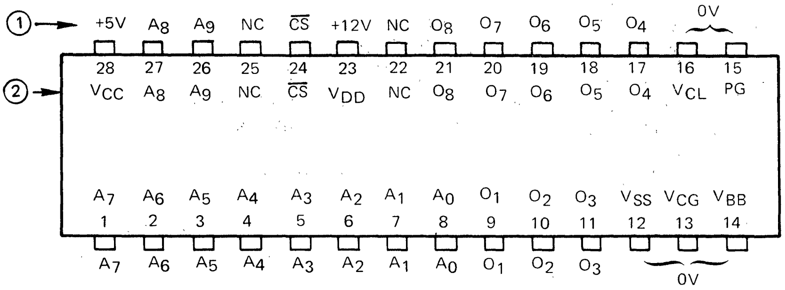
② All voltages relative to VSS = 0V.

PACKAGE OUTLINE μPD458D

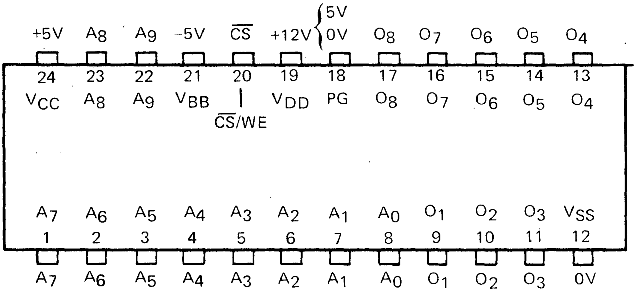


ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.41 MAX.
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0 004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

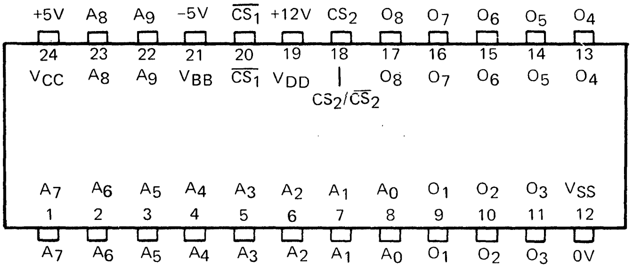
μPD458



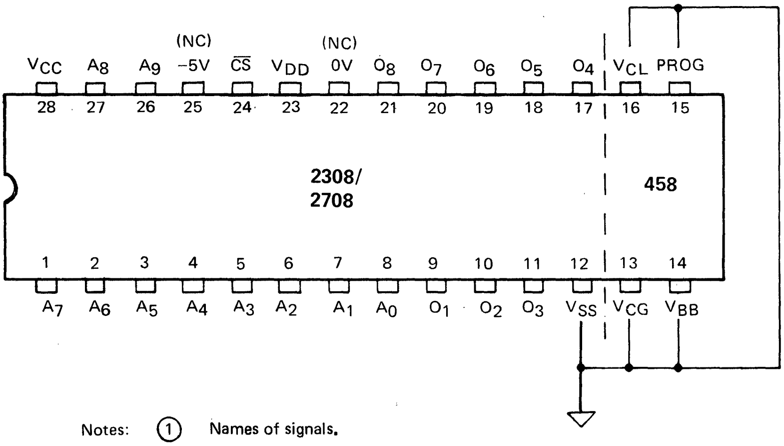
μPD458D (EEPROM)



2708 (PROM ERASABLE WITH ULTRAVIOLET)



μPD2308C/D – 2308 (MASK ROM)



COMMON PIN CONFIGURATION

Notes: ① Names of signals.
② Names of the terminal.

NEC Microcomputers, Inc.

NEC
μPD2716
PRELIMINARY

16K ULTRAVIOLET ERASABLE PROM

DESCRIPTION

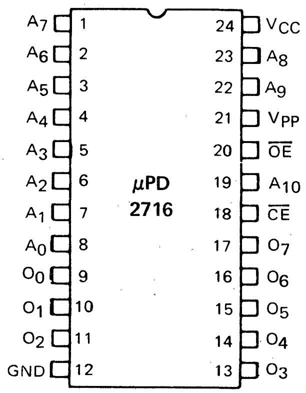
The μPD2716 is a 16,384-bit Ultraviolet Erasable and Electrically Programmable Read Only Memory. Organized as 2048 words x 8 bits, it operates from a single +5 volt powe supply, making it ideal for microprocessor applications. It is pin-for-pin compatible with the μPD2316E, allowing economical changeover to a masked ROM for production quantities.

The μPD2716 features fast, simple, one pulse programming, controlled by TTL level signals. Total programming time for all 16,384 bits is only 100 seconds.

FEATURES

- Access Time – 450 ns Max
- 2048 Words x 8 Bits Organization
- Single +5V Supply
- Pin Compatible with μPD2316E Masked ROM
- Fast Programming
- TTL Level Controls for Reading and Programming
- Available in a 24 Pin Ceramic Package

PIN CONFIGURATION



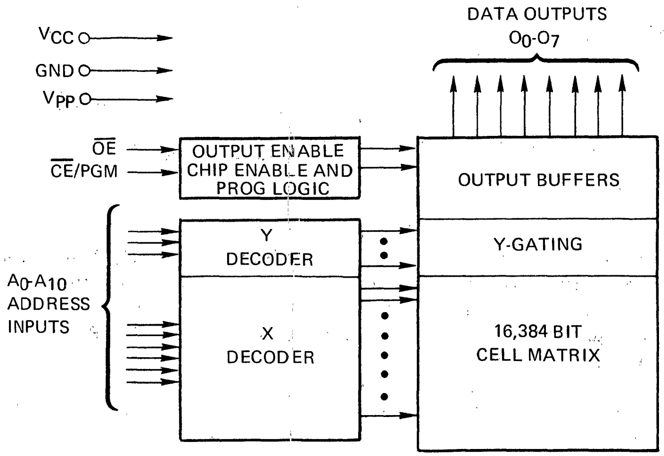
PIN NAMES

A_0-A_9	Addresses
$\overline{CE}$/PGM	Chip Enable/Program
$\overline{OE}$	Output Enable
O_0-O_7	Outputa

MODE SELECTION

PINS MODE	$\overline{CE}$/PGM	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages	+6 to −0.3 Volts ①
All Output Voltages	+6 to −0.3 Volts ①
Supply Current V_{PP}	+26.5 to −0.3 Volts ②

Notes: ① With Respect to Ground.

② With Respect to Ground During Program.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$*T_a = 25°C$

CAPACITANCE ①

$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}		4	6	pF	$V_{IN} = 0V$
Output Capacitance	C_{OUT}		8	12	pF	$V_{OUT} = 0V$

Note: ① This parameter is only sampled and is not 100% tested.

ERASURE OPERATION

The recommended erasure procedure is to illuminate the window with a ultraviolet lamp which has a wavelength of 2537 angstroms (Å). The distance should be one inch from the window to the lamp. Erasure time will be from 19 to 45 minutes depending on the type of ultraviolet lamp. The amount of time required can be expressed as the total amount of ultraviolet energy incident to the window, expressed in watt-seconds per square centimeter. The μPD2716 requires an integrated dosage (ultraviolet intensity x exposure time) of 15 watt-seconds/cm^2. This erase energy includes sufficient guard-band to ensure complete erasure of all bits.

READ OPERATION

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%; ① ② ; V_{PP} = V_{CC} ± 0.6V ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP④	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}			10	µA	V_{IN} = 5.25V
Output Leakage Current	I_{LO}			10	µA	V_{OUT} = 5.25V
Vpp Current	I_{PP1} ②			12	mA	V_{PP} = 5.85V
V_{CC} Current (Standby)	I_{CC1} ②		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
V_{CC} Current (Active)	I_{CC2} ②		57	100	mA	$\overline{CE}$ = $\overline{CE}$ = V_{IL}
Input Low Voltage	V_{IL}	-0.1		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH}	2.2			V	I_{OH} = -400µA

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5% ① ② ; V_{PP} = V_{CC} ± 0.6V ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP④	LIMITS MAX	UNIT	TEST ⑥ CONDITIONS
Address to Output Delay	t_{ACC}			450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}			450	ns	$\overline{OE}$ = V_{IL}
Output Enable to Output Delay	t_{OE}			140	ns	$\overline{CE}$ = V_{IL}
Output Enable High to Output Float	t_{DF}	0		100	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold	t_{OH}	0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Notes: ① V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.

② Vpp may be connected directly to V_{CC} except during programming. The supply current would then be the sum of ICC and I_{PP1}.

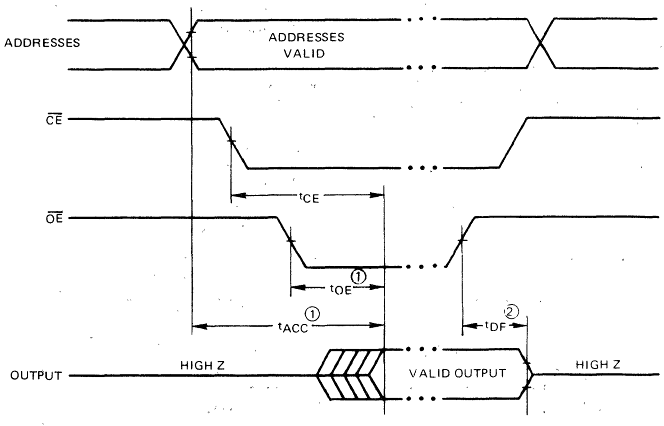
③ The tolerance of 0.6V allows the use of a driver circuit for switching the Vpp supply pin from V_{CC} in read to 25V for programming.

④ Typical values are for T_a = 25°C and nominal supply voltages.

⑤ This parameter is only sampled and is not 100% tested.

⑥ AC Test Conditions: Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs: 1V and 2V
Outputs: 0.8V and 2V

TIMING WAVEFORMS ①



Notes: ① $\overline{OE}$ may be delayed up to t_{ACC} − t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING OPERATION

Initially, and after each erasure, all bits of the μPD2716 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The μPD2716 is programmed by applying a 50 ms, TTL programming pulse to the $\overline{CE}$/PGM pin with the $\overline{CE}$ input high and the V_{PP} supply at 25V ± 1V. Any location may be programmed at any time – either individually, sequentially, or randomly. The programming time for a single bit is only 50 ms and for all bits is approximately 100 seconds for the μPD2716.

CAUTION: The V_{CC} and V_{PP} supplied must be sequenced on and off such that V_{CC} is applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} to prevent damage to the μPD2716. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26V maximum specification. For convenience in programming, the μPD2716 may be verified with the V_{PP} supply at 25V ± 1V. During normal read operation, however, V_{PP} must be at V_{CC}.

DC CHARACTERISTICS ①

$T_a = 25°C \pm 5°C$; $V_{CC} = 5V \pm 5\%$ ②; $V_{PP} = 25V \pm 1V$ ② ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current (for Any Input)	I_{LI}			10	μA	V_{IN} = 5.25V/0.45
V_{PP} Supply Current	I_{PP1}			12	mA	$\overline{CE}$/PGM = V_{IL}
V_{PP} Supply Current During Programming Pulse	I_{PP2}			30	mA	$\overline{CE}$/PGM = V_{IH}
V_{CC} Supply Current	I_{CC}			100	mA	
Input Low Level	V_{IL}	0.1		0.8	V	
Input High Level	V_{IH}	2.0		V_{CC} + 1	V	

AC CHARACTERISTICS ①

$T_a = 25°C \pm 5°C$; $V_{CC} = 5V \pm 5\%$ ②; $V_{PP} = 25V \pm 1V$ ② ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS④
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	$\overline{CE}$/PGM = V_{IL}
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}$/PGM = V_{IL}
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	5			ns	
Program Pulse Fall Time	t_{PFT}	5			ns	

Notes: ① NEC Microcomputer's standard product warranty applies only to devices programmed to specifications described herein.

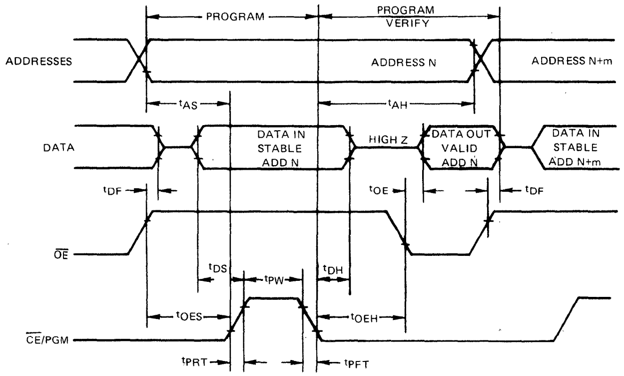
② V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The μPD2716 must not be inserted into or removed from a board with V_{PP} at 25 ± 1V to prevent damage to the device.

③ The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

④ AC Test Conditions:

V_{CC}	5V ± 5%	Input Pulse Levels	0.8V to 2.2V
V_{PP}	25V ± 1V	Input Timing Reference Level	1V and 2V
Input Rise and Fall Times (10% to 90%)	20 ns	Output Timing Reference Level	0.8V and 2V

TIMING WAVEFORM



SP2716-9-78-GY-CAT

NEC Microcomputers, Inc.

NEC

μPD2316E

FULLY DECODED 16,384 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

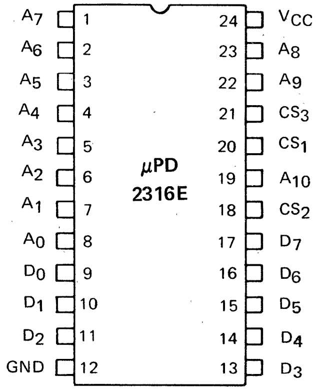
The NEC μPD2316E is a high speed 16,384 bit mask programmable Read Only Memory organized as 2048 words by 8 bits. The μPD2316E is fabricated with N-channel MOS technology.

The inputs and outputs are fully TTL compatible. The device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and desired chip select code is fixed during the masking process.

FEATURES

- Access Time 450 ns Max
- 2048 Words x 8 Bits Organization
- Single +5V ±10% Power Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Three Programmable Chip Select Inputs for Easy Memory Expansion
- Three-State Output – OR-Tie Capability
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Direct Replacement for 2316E
- Available in 24-pin plastic or ceramic packages

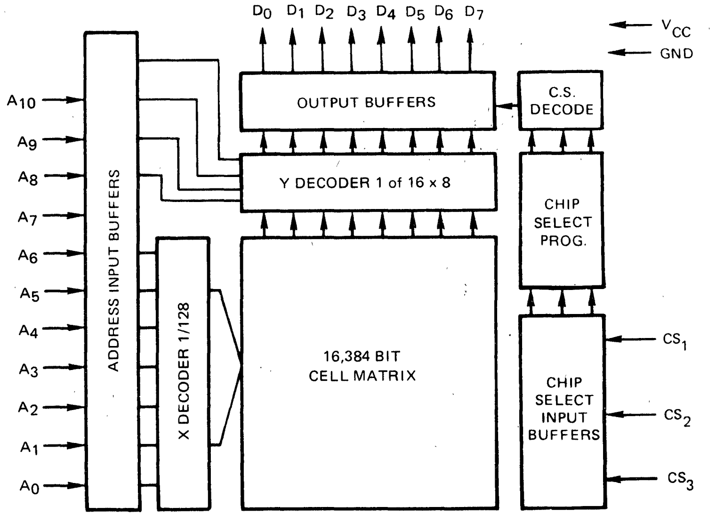
PIN CONFIGURATION



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$D_1 - D_8$	Data Outputs
$CS_1 - CS_3$	Programmable Chip Select Inputs

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7.0 Volts ①

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5 ± 5% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ①	MAX		
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	V_{IN} = 0V
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Output Leakage Current	I_{LOL}			−20	μA	Chip Deselected, V_O = 0V
Power Supply Current	I_{CC}		70	120	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	+2.4		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output "High" Voltage	V_{OH}	+2.4			V	I_{OH} = −400 μA

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

CAPACITANCE

$T_a = 25^\circ C$; f = 1 MHz

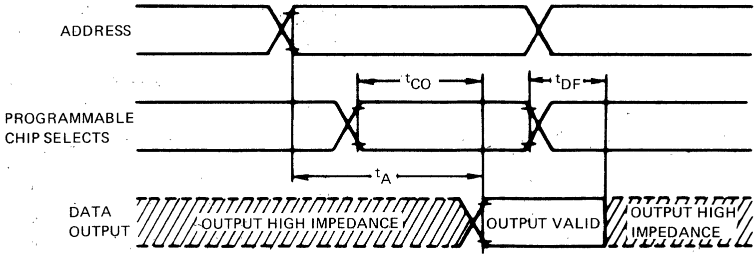
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	10	pf	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}		10	15	pf	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

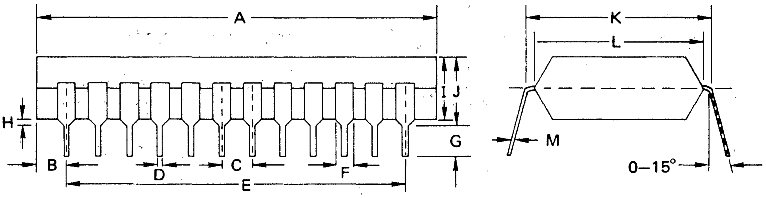
$T_a = -10^\circ C$ to $+70^\circ C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	$t_T = t_r = t_f = 20$ ns $V_{ref\ in} = 1V, 2.2V$ $V_{ref\ out} = 0.8V, 2V$ Output LOAD = 1 TTL GATE $C_L = 100$ pf
Chip Select to Output Enable Delay Time	t_{CO}			120	ns	
Chip Deselect to Output Data Float Delay Time	t_{DF}	10		100	ns	

TIMING WAVEFORMS

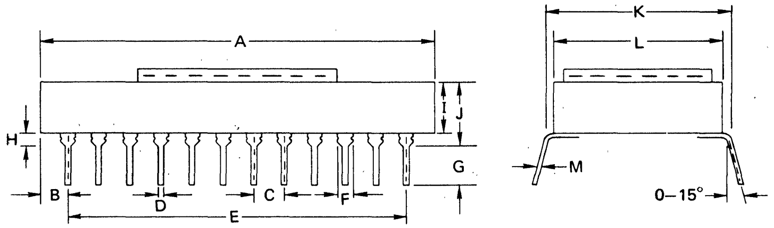


PACKAGE OUTLINE
μPD2316EC/D



μPD2316EC (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25\ ^{+0.10}_{-0.05}$	$0.01\ ^{+0.004}_{-0.0019}$



μPD2316ED (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

SP2316E-9-78-GY-CAT

FULLY DECODED 32,768 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

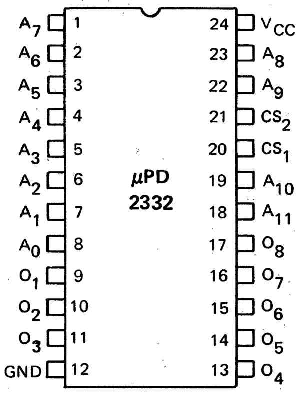
The NEC μPD2332 is a Fully Decoded 32,768 Bit Mask Programmable Read-Only Memory organized as 4,096 Words by 8 Bits. The μPD2332 has two chip select inputs and the combination of "High"/"Low" levels of these inputs is mask-programmable.

The μPD2332 is fabricated with sophisticated N-channel MOS technology and features high speed and TTL compatibility for simple interface with bipolar circuits.

FEATURES

- 4096 Words x 8 Bits Organization
- Directly TTL Compatible – All Inputs and Outputs
- Fully Static (No Clock or Refresh Required)
- Single +5V Power Supply
- High Speed – Access Time 450 ns Max.
- Three-State Output – OR-Tie Capability
- Two Programmable Chip Select Inputs for Easy Memory Expansion
- N-Channel MOS Technology
- Pin Compatible with TI TMS4732
- 24 Pin Plastic or Ceramic Dual-in-Line Package

PIN CONFIGURATION



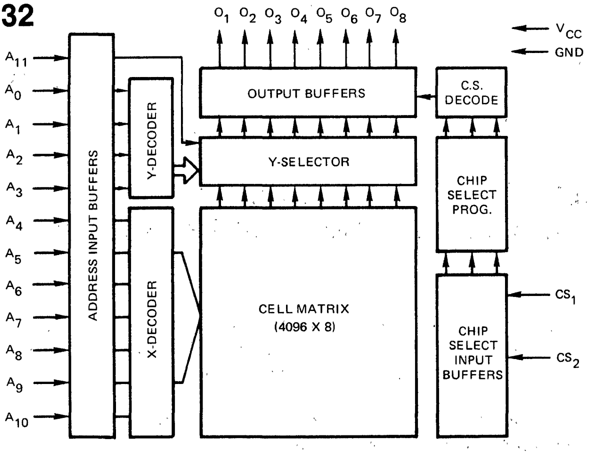
PIN NAMES

$A_0 - A_{11}$	Address Inputs
$O_1 - O_8$	Data Outputs
$CS_1 - CS_2$	Programmable Chip Select Inputs

When ordering the μPD2332, specify a chip select combination of CS_1 and CS_2 from the following.

CS_2	CS_1
0	0
0	1
1	0
1	1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . −10°C to +70°C
Storage Temperature . . . . −65°C to +125°C
Supply Voltage On Any Pin . . . . −0.5 to +7.0 Volts①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$*T_a = 25°C$

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN.	TYP.①	MAX.	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	
Output Leakage Current	I_{LOH}			+10	μA	CS = 2.2V (Deselected) $V_{OUT} = V_{CC}$
Output Leakage Current	I_{LOL}			−10	μA	CS = 2.2V (Deselected) V_{OUT} = 0V
Power Supply Current	I_{CC}		55	110	mA	All inputs 5.25V Data Out Open
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = −100 μA

Note: ① Typical Values for $T_a = 25°C$ and nominal supply voltages.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

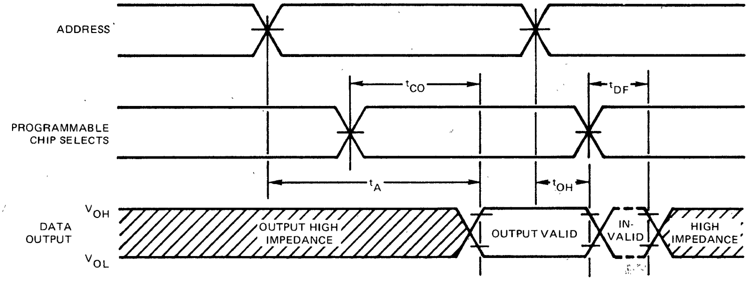
PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

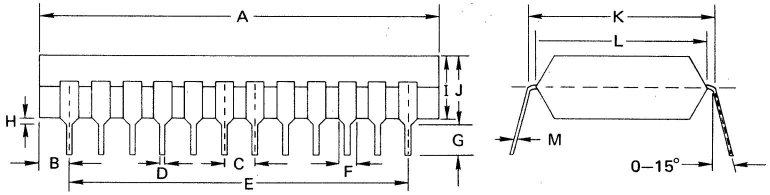
$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	$t_T = t_r = t_f$ = 20 ns
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	C_L = 100 pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	Load = 1TTL gate
Output Hold Time	t_{OH}	20			ns	V_{IN} = 0.8 to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.45/2.2V

TIMING WAVEFORMS

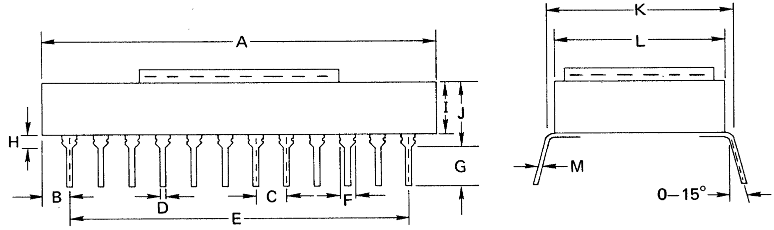


PACKAGE OUTLINE μPD2332C/D



μPD2332C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2332D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

NEC Microcomputers, Inc.

NEC
μPD2364

FULLY DECODED 65,536 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

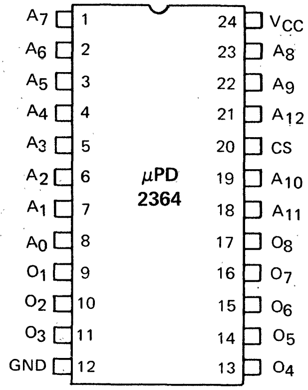
The NEC μPD2364 is a high speed 65,536 bit mask programmable Read Only Memory organized as 8,192 words by 8 bits. The μPD2364 is fabricated with N-channel MOS technology.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The chip select input is programmable. Any of active high or low level chip select input can be defined and desired chip select code is fixed during the masking process.

FEATURES

- 8,192 Words x 8 Bits Organization
- Directly TTL Compatible — All Inputs and Outputs
- Single +5V Power Supply
- High Speed — Access Time 450 ns Max.
- Three-State Output — OR-Tie Capability
- One Programmable Chip Select Input for Easy Memory Expansion
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Pin Compatible with MK36000
- Available in 24 Pin Ceramic or Plastic Dual-in-Line Package

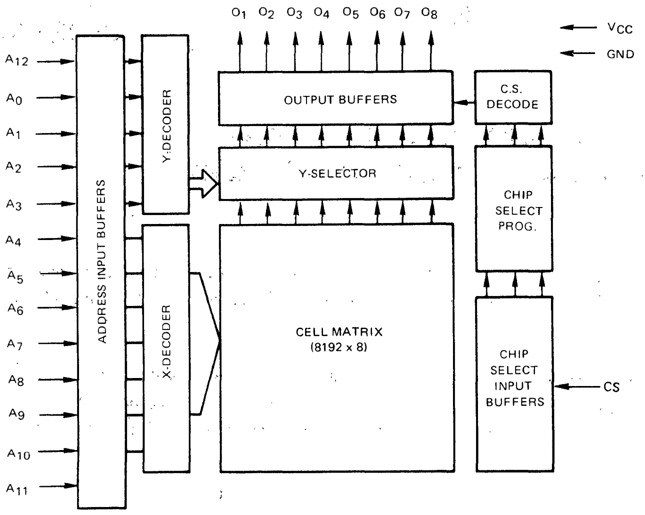
PIN CONFIGURATION



PIN NAMES

$A_0 - A_{12}$	Address Inputs
$O_1 - O_8$	Data Outputs
CS	Programmable Chip Select Input

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage On Any Pin	−0.5 to +7.0 Volts ①

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ①	MAX		
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	$V_{IN} = 0V$
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Output Leakage Current	I_{LOL}			−10	μA	Chip Deselected, $V_O = 0V$
Power Supply Current	I_{CC}		80	140	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output "High" Voltage	V_{OH}	2.2			V	$I_{OH} = -400$ μA

Note: ① Typical Values for $T_a = 25°C$ and nominal supply voltages.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

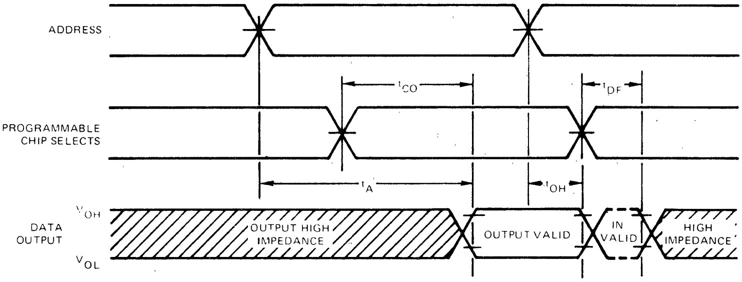
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

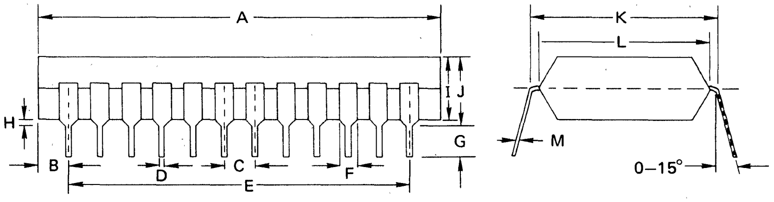
$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address to Output Delay Time	t_A			450	ns	$t_T = t_r = t_f = 20$ ns
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	$C_L = 100$ pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	Load = 1TTL gate
Output Hold Time	t_{OH}	20			ns	$V_{IN} = 0.8$ to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.8 to 2.0V

TIMING WAVEFORMS

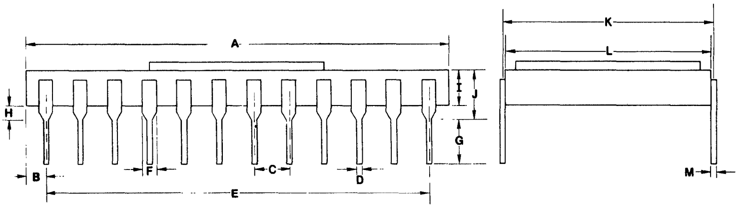


PACKAGE OUTLINE
μPD2364C/D



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25\ ^{+0.10}_{-0.05}$	$0.01\ ^{+0.004}_{-0.0019}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	30.78 Max	1.21 Max
B	1.42	0.06
C	2.54	0.10
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94	1.10
F	1.02	0.04
G	3.2 Min	0.13 Min
H	1.02	0.04
I	3.23	0.13
J	4.25 Max	0.17 Max
K	15.24	0.60
L	14.93	0.59
M	0.25 ± 0.05	0.010 ± 0.002

NOTES

MICROCOMPUTER INDEX

μCOM-4

μCOM-8

Processors

Single Chip Microcomputers

Peripherals

Microcomputer on a Board

μCOM-4 MICROCOMPUTER SELECTION GUIDE

DEVICE	PRODUCT	ROM	RAM	I/O	TECHNOLOGY	OUTPUT	SUPPLY VOLTAGES	PINS
μPD548	μCOM-42 CPU	1920 x 10	96 x 4	35	PMOS	–35V, O.D.	–10	42
μPD546	μCOM-43 CPU	2000 x 8	96 x 4	35	PMOS	–10V, O.D.	–10	42
μPD553	μCOM-43H CPU	2000 x 8	96 x 4	35	PMOS	–35V, O.D.	–10	42
μPD650	μCOM-43C CPU	2000 x 8	96 x 4	35	CMOS	push-pull	+5	42
μPD547	μCOM-44 CPU	1000 x 8	64 x 4	35	PMOS	–10V, O.D.	–10	42
μPD547L	μCOM-44L CPU	1000 x 8	64 x 4	35	PMOS	–10V, O.D.	–8	42
μPD552	μCOM-44H CPU	1000 x 8	64 x 4	35	PMOS	–35V, O.D.	–10	42
μPD651	μCOM-44C CPU	1000 x 8	64 x 4	35	CMOS	push-pull	+5	42
μPD550	μCOM-45 CPU	640 x 8	32 x 4	21	PMOS	–35V, O.D.	–10	28
μPD554	μCOM-45 CPU	1000 x 8	32 x 4	21	PMOS	–35V, O.D.	–10	28
μPD652	μCOM-45C CPU	1000 x 8	32 x 4	21	CMOS	push-pull	+5	28
μPD551	μCOM-46 CPU with A/D	1000 x 8	64 x 4	28	PMOS	–10V, O.D.	–10	40
μPD555	μCOM-42 EVACHIP	–	96 x 4	35	PMOS	–10V, O.D.	–10	64
μPD556	μCOM-43 EVACHIP	–	96 x 4	35	PMOS	–10V, O.D.	–10	64

Notes: O.D. = Open Drain
H = High Negative Voltage Outputs
C = CMOS
L = Low Power

μCOM-8 MICROCOMPUTER SELECTION GUIDE

MICROPROCESSORS

DEVICE	PRODUCT	SIZE	TECHNOLOGY	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD780	Microprocessor	8-bit	NMOS	3-State	2.5 MHz	+5	40
μPD780-1	Microprocessor	8-bit	NMOS	3-State	4.0 MHz	+5	40
μPD8085A	Microprocessor	8-bit	NMOS	3-State	3.0 MHz	+5	40
μPD8080AF	Microprocessor	8-bit	NMOS	3-State	2.0 MHz	+12 ± 5	40
μPD8080AF-2	Microprocessor	8-bit	NMOS	3-State	2.5 MHz	+12 ± 5	40
μPD8080AF-1	Microprocessor	8-bit	NMOS	3-State	3.0 MHz	+12 ± 5	40

SINGLE CHIP MICROCOMPUTERS

DEVICE	PRODUCT	ROM	RAM	I/O	TECHNOLOGY	SIZE	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD8021	Microcomputer	1024 x 8	64 x 8	21	NMOS	8-bit	3-State	3 MHz	+5	28
μPD8035	Microcomputer	External	64 x 8	27	NMOS	8-bit	3-State	6 MHz	+5	40
μPD8039	Microcomputer	External	128 x 8	27	NMOS	8-bit	3-State	6 MHz	+5	40
μPD8041	Microcomputer	1024 x 8	64 x 8	18	NMOS	8-bit	3-State	6 MHz	+5	40
μPD8048	Microcomputer	1024 x 8	64 x 8	27	NMOS	8-bit	3-State	6 MHz	+5	40
μPD8049	Microcomputer	2048 x 8	128 x 8	27	NMOS	8-bit	3-State	6 MHz	+5	40
μPD8741	Microcomputer	1024 x 8 (UV)	64 x 8	18	NMOS	8-bit	3-State	6 MHz	+5	40
μPD8748	Microcomputer	1024 x 8 (UV)	64 x 8	27	NMOS	8-bit	3-State	6 MHz	+5	40

μCOM-8 MICROCOMPUTER SELECTION GUIDE

SYSTEM SUPPORT

DEVICE	PRODUCT	SIZE	TECHNOLOGY	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD371	Tape Cassette Controller	8-bit	NMOS	3-State	2 MHz	+12 ± 5	42
μPD372	Floppy Disk Controller	8-bit	NMOS	3-State	2 MHz	+12 ± 5	42
μPD379	Synchronous Receiver/ Transmitter	8-bit	NMOS	3-State	800K baud	+12 ± 5	42
μPD765	Double Sided/Double Density Floppy Disk Controller	8-bit	NMOS	3-State	8 MHz	+5	40
μPD8155	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPD8156	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPB8212	I/O Port	8-bit	Bipolar	3-State	–	+5	24
μPD8214	Priority Interrupt Controller	3-bit	Bipolar	Open Collector	3 MHz	+5	24
μPB8216	Bus Driver Non-Inverting	4-bit	Bipolar	3-State	–	+5	16
μPB8224	Clock Generator Driver	2 phase	Bipolar	High Level Clock	3 MHz	+12 ± 5	16
μPB8226	Bus Driver Inverting	4-bit	Bipolar	3-State	–	+5	16
μPB8228	System Controller	8-bit	Bipolar	3-State	–	+5	28
μPB8238	System Controller	8-bit	Bipolar	3-State	–	+5	28
μPD8243	I/O Expander	4 x 4 bits	NMOS	3-State	–	+5	24
μPD8251	Programmable Communications Interface (Async/Sync)	8-bit	NMOS	3-State	A-9.6K baud S-56K baud	+5	28
μPD8251A	Programmable Communications Interface (Async/Sync)	8-bit	NMOS	3-State	A-9.6K baud S-64K baud	+5	28
μPD8253	Programmable Timer	8-bit	NMOS	3-State	3.3 MHz	+5	24
μPD8253-5	Programmable Timer	8-bit	NMOS	3-State	3.3 MHz	+5	24
μPD8255	Peripheral Interface	8-bit	NMOS	3-State	–	+5	40
μPD8255A-5	Peripheral Interface	8-bit	NMOS	3-State	–	+5	40
μPD8257	Programmable DMA Controller	8-bit	NMOS	3-State	3 MHz	+5	40
μPD8257-5	Programmable DMA Controller	8-bit	NMOS	3-State	3 MHz	+5	40
μPD8259	Programmable Interrupt Controller	8-bit	NMOS	3-State	–	+5	28
μPD8259-5	Programmable Interrupt Controller	8-bit	NMOS	3-State	–	+5	28
μPD8279-5	Programmable Keyboard/ Display Interface	8-bit	NMOS	3-State	–	+5	40
μPD8355	2048 x 8 ROM with I/O Ports	8-bit	NMOS	3-State	–	+5	40
μPD8755A	2048 x 8 EPROM with I/O Ports	8-bit	NMOS	3-State	–	+5	40

μCOM-8 MICROCOMPUTER SELECTION GUIDE

MEMORY SUPPORT

DEVICE	PRODUCT	SIZE	TECHNOLOGY	OUTPUT	ACCESS TIME	SUPPLY VOLTAGES	PINS
μPD2316E	Mask ROM	2048 x 8	NMOS	3-State	450 ns	+5	24
μPD2332	Mask ROM	4096 x 8	NMOS	3-State	450 ns	+5	24
μPD2364	Mask ROM	8192 x 8	NMOS	3-State	450 ns	+5	24
μPD454	Electrically Erasable Programmable ROM	256 x 8	NMOS	3-State	800 ns	+12 + 5*	24
μPD458	Electrically Erasable Programmable ROM	1024 x 8	NMOS	3-State	450 ns	+12 + 5*	28
μPD2716	UV Erasable Programmable ROM	2048 x 8	NMOS	3-State	450 ns	+5	24
μPD411	Dynamic RAM	4096 x 1	NMOS	3-State	150–350 ns	+12 ± 5	22
μPD411A	Dynamic RAM	4096 x 1	NMOS	3-State	200–350 ns	+12 ± 5	22
μPD416	Dynamic RAM	16384 x 1	NMOS	3-State	120–350 ns	+12 ± 5	16
μPD2101AL	Static RAM	256 x 4	NMOS	3-State	250–450 ns	+5	22
μPD2102AL	Static RAM	1024 x 1	NMOS	3-State	250–450 ns	+5	16
μPD2111AL	Static RAM	256 x 4	NMOS	3-State	250–450 ns	+5	18
μPD2114L	Static RAM	1024 x 4	NMOS	3-State	200–450 ns	+5	18
μPD4104	Static RAM	4096 x 1	NMOS	3-State	85–300 ns	+5	18
μPD421	Static RAM	1024 x 8	NMOS	3-State	85–100 ns	+5	22
μPD443/6508	Static RAM	1024 x 1	CMOS	3-State	200 ns	+5	16
μPD5101L	Static RAM	256 x 4	CMOS	3-State	450–800 ns	+5	22
μPD444/6514	Static RAM	1024 x 4	CMOS	3-State	300 ns	+5	18
μPD445L	Static RAM	1024 x 4	CMOS	3-State	450–650 ns	+5	20

Note: * – Read Mode

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
AMD	AM8080A/9080A	Microprocessor (2.0 MHz)	μPD8080AF
	AM8080A-2/9080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	AM8080A-1/9080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	AM8085A	Microprocessor (3.0 MHz)	μPD8085A
	AM8155	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155
	AM8156	Programmable Peripheral Interface with 256 x 8 RAM	μPD8156
	AM8212	I/O Port (8-Bit)	μPB8212
	AM8214	Priority Interrupt Controller	μPB8214
	AM8216	Bus Driver, Inverting	μPB8216
	AM8224	Clock Generator/Driver	μPB8224
	AM8226	Bus Driver, Non-Inverting	μPB8226
	AM8228	System Controller	μPB8228
	AM8238	System Controller	μPB8238
	AM8251	Programmable Communications Interface	μPD8251
	AM8255	Programmable Peripheral Interface	μPD8255
	AM8257	Programmable DMA Controller	μPD8257
	AM8355	Programmable Peripheral Interface with 2048 x 8 ROM	μPD8355
	AM8048	Single Chip Microcomputer	μPD8048
INTEL	8080A	Microprocessor (2.0 MHz)	μPD8080AF
	8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	8021	Microcomputer with ROM	μPD8021
	8035	Microprocessor	μPD8035
	8039	Microprocessor	μPD8039
	8041	Programmable Peripheral Controller with ROM	μPD8041
	8048	Microcomputer with ROM	μPD8048
	8049	Microcomputer with ROM	μPD8049
	8085	Microprocessor	μPD8085A
	8155	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155
	8156	Programmable Peripheral Interface with 256 x 8 RAM	μPD8156
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8224	Clock Generator/Driver	μPB8224
	8226	Bus Driver, Inverting	μPB8226
	8228	System Controller	μPB8228
	8238	System Controller	μPB8238
	8243	I/O Expander	μPD8243

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
INTEL (CONT.)	8251	Programmable Communications Interface (Async/Sync)	μPD8251
	8251A	Programmable Communications Interface (Async/Sync)	μPD8251A
	8253	Programmable Timer	μPD8253
	8253-5	Programmable Timer	μPD8253-5
	8255	Programmable Peripheral Interface	μPD8255
	8255A	Programmable Peripheral Interface	μPD8255A-5
	8255A-5	Programmable Peripheral Interface	μPD8255A-5
	8257	Programmable DMA Controller	μPD8257
	8257-5	Programmable DMA Controller	μPD8257-5
	8259	Programmable Interrupt Controller	μPD8259
	8259-5	Programmable Interrupt Controller	μPD8259-5
	8279-5	Programmable Keyboard/Display Interface	μPD8279-5
	8355	Programmable Peripheral Interface with 2048 x 8 ROM	μPD8355
	8741	Programmable Peripheral Controller with EPROM	μPD8741
	8748	Microcomputer with EPROM	μPD8748
	8755A	Programmable Peripheral Interface with 2K x 8 EPROM	μPD8755A
NATIONAL	INS8080A	Microprocessor (2.0 MHz)	μPD8080AF
	INS8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	INS8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8224	Clock Generator/Driver	μPB8224
	8226	Bus Driver, Inverting	μPB8226
	8228	System Controller	μPB8228
	8238	System Controller	μPB8238
	INS8251	Programmable Communications Interface	μPD8251
	INS8253	Programmable Timer	μPD8253
	INS8255	Programmable Peripheral Interface	μPD8255
	INS8257	Programmable DMA Controller	μPD8257
	INS8259	Programmable Interrupt Controller	μPD8259
T.I.	TMS8080A	Microprocessor (2.0 MHz)	μPD8080AF
	TMS8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	TMS8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	SN74S412	I/O Port (8-Bit)	μPB8212
	SN74LS424	Clock Generator/Driver	μPB8224
	SN74S428	System Controller	μPB8228
	SN74S438	System Controller	μPB8238

NEC Microcomputers, Inc.

μCOM-42 4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μCOM-42 (Part No. μPD548) is a single chip microcomputer that is ideally suited for Electronic Cash Register (ECR), Point of Sale (POS) and Electronic Scale applications.

Containing a 4-bit Parallel ALU, ROM for program storage and RAM for data storage, the μCOM-42 provides an economical and simple solution to many Vending/Calculating requirements.

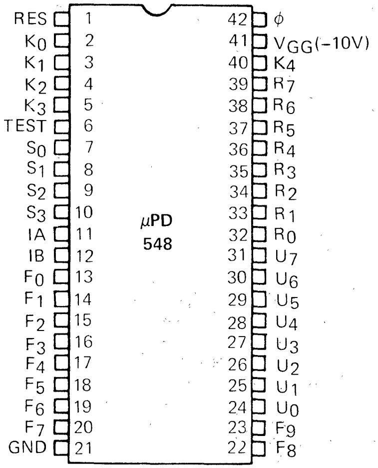
Because of its extensive instruction set and five input/output ports, the μCOM-42 is capable of controlling an 8 x 4 keyboard, an 8 digit display and low cost ECR-type printers.

Finally, the on-chip RAM space can be augmented by an external CMOS RAM for applications requiring low power data retention.

FEATURES

- Stand Alone 4-bit Microcomputer
- All 72 Instructions are Single Byte
- 10 μsec Instruction Cycle
- 1920 x 10-Bit Program Memory (ROM)
- 96 x 4-Bit Data Memory (RAM)
- 4-Level Stack
- 2 Interrupt Request Lines
- I/O Compatible with TTL
- 10 Discrete Output Ports (F_0-F_9)
- Two 8-Bit Output Ports (U_0-U_7, R_0-R_7)
- One 4-Bit Input Port (K_0-K_3)
- One 4-Bit Input/Output Port (S_0-S_3)
- One Single Bit Testable Input Port (K_4)
- Single Phase TTL Level Clock (200 KHz Max.)
- Single Supply, −10V PMOS Technology
- 42 Pin Plastic Dual-in-Line Package

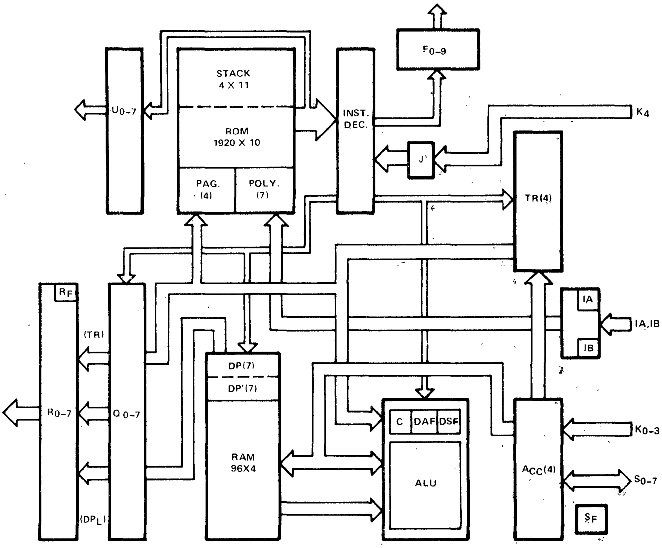
PIN CONFIGURATION



PIN NAMES

RES	Reset
K_0–K_3	Input Port K
TEST	Input for Testing (Normally V_{GG})
S_0–S_3	Input/Output Port S
IA, IB	Interrupt Input Ports
F_0–F_9	Output Port F
U_0–U_7	Output Port U
R_0–R_7	Output Port R
K_4	Input Port for Condition Test
φ	Clock Input

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Program Counter

The 11-bit program counter is composed of two sections, a 4-bit page register and a 7-bit polynomial counter. The page register selects one page out of 15, each consisting of 128 words addressed by the 7-bit polynomial counter. The contents of the page register are independent of the operation of the polynomial counter, so that it is not affected by polynomial counter overflow.

Stack Register

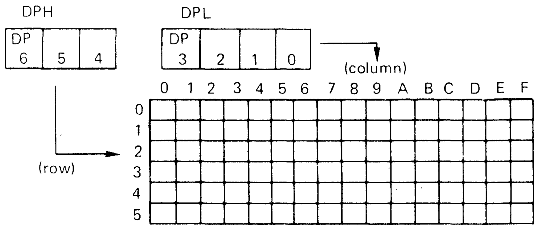
In order to store the program counter contents upon an interrupt or subroutine call, four 11-bit stack registers are provided to enable a combination of subroutine calls and interrupt nesting to four levels. The stack register is a LIFO (Last in, First-Out) type.

ROM (Read Only Memory)

The on-chip ROM consists of 1,920 words of ten bits each and is divided into 15 pages. A page is selected by the page register, the upper four bits of the program counter. Each page consists of 128 words addressed by the polynomial counter, the lower seven bits of the program counter.

RAM (Data Memory)

The data memory is a 96 x 4-bit RAM addressed by a 7-bit data pointer (DP). The RAM is divided into six rows of 16 4-bit columns each. The 7-bit data pointer consists of an upper 3-bit register (DPH) which selects the row address and a lower 4-bit register (DPL) which selects the column address.



Data memory (96 x 4)

FUNCTIONAL DESCRIPTION (CONT.)

Internal Registers

The Accumulator (ACC) is connected with the ALU and the carry flip-flop (C) and is able to perform either binary or decimal arithmetic by testing the decimal addition flip-flop (DAF) and the decimal subtraction flip-flop (DSF). Constants are loaded into the ACC as immediate data from ROM and variable data are loaded from or exchanged with RAM. The ACC is also connected with the temporary register (TR), the parallel I/O port S and the parallel input port K. The TR is an auxiliary register used for temporary storage of 4-bit data. The Q register is an 8-bit serial-in/parallel-out shift register designed for display digit strobing and generation of printer hammer triggers.

I/O Ports

The R port is an 8-bit parallel port that may be loaded from the Q register for digit strobing or loaded with the 4-bit TR and the 4-bit DPL for external RAM addressing. The U port is an 8-bit parallel port that is loaded with immediate data. It is usually used for outputting segment information for display and digit information for key scanning. The K port is a 4-bit input port that is usually used for key scan input. The K4 port is a single bit port that is testable by software. The S port is a 4-bit parallel I/O port that is typically used as the data bus to external RAM. The F port consists of ten discrete output lines that can be individually set or reset under program control.

Interrupt Ports

Two interrupt input lines, IA and IB, are available to accept an interrupt request when interrupts are enabled. IA has a higher priority level than IB. Thus when concurrent interrupts occur on both IA and IB only the IA interrupt is accepted and both are disabled. But a single IB interrupt disables only the IB interrupt and leaves IA enabled.

INSTRUCTION SET

The μCOM-42 has a powerful 72, 10-bit word, instruction set. All instructions are single words. There are a number of multi-function instructions which reduce the number of program steps. In addition, automatic data pointer modification, single word subroutine calls and N-way branch capability all help improve operation speed and reduce ROM requirements. The μCOM-42 instruction set is summarized below.

MNEMONIC	CYCLES	DESCRIPTION	CONDITIONS FOR SKIP
CMA	1	$A_{CC} \leftarrow (\overline{A_{CC}})$	
CIA	1	$A_{CC} \leftarrow (\overline{A_{CC}}) + 1$	
INA	1/2	$A_{CC} \leftarrow (A_{CC}) + 1$	Carry = 1
DEA	1/2	$A_{CC} \leftarrow (A_{CC}) - 1$	Borrow ≠ 1
RFC	1	$C \leftarrow 0$	
SFC	1	$C \leftarrow 1$	
DSM	1	Decimal Subtract Mode	
DAM	1	Decimal Add Mode	
AD	1/2	$A_{CC} \leftarrow (A_{CC}) + [DP]$	Carry = 1
ADC	1	$A_{CC}, C \leftarrow (A_{CC}) + [DP] + (C)$	
ADI	1/2	$A_{CC} \leftarrow (A_{CC}) + I_3 I_2 I_1 I_0$	Carry = 1
LM	1	$A_{CC} \leftarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2 M_1 M_0$	
XM	1	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2 M_1 M_0$	
XMI	1/2	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2 M_1 M_0$ $DP_L \leftarrow (DP_L) + 1$	$(DP_L) = 8$ or $(DP_L) = 0$
XMD	1/2	$(A_{CC}) \leftrightarrow [DP]$, $DP_H \leftarrow (DP_H)$ $M_2 M_1 M_0$, $DP_L \leftarrow (DP_L) - 1$	$(DP_L) = F$ or $(DP_L) = 7$
LI	1	$A_{CC} \leftarrow I_3 I_2 I_1 I_0$	
LDI	1	$DP \leftarrow I_6 - I_0$	
IND	1/2	$DP_L \leftarrow (DP_L) + 1$	$(DP_L) = 8$ or $(DP_L) = 0$
DED	1/2	$DP_L \leftarrow (DP_L) - 1$	$(DP_L) = F$ or $(DP_L) = 7$
XDP	1	$(DP) \leftrightarrow (DP')$	
ZAG	1	$000DP_L \leftarrow (DP)$	

INSTRUCTION SET

MNEMONIC	CYCLES	DESCRIPTION	CONDITIONS FOR SKIP
XTA	1	$(A_{CC}) \leftrightarrow (TR)$	
LTI	1	$TR \leftarrow I_3\ I_2\ I_1\ I_0$	
QS1	1	$Q_{n+1} \leftarrow Q_n,\ Q_0 \leftarrow 1$	
QS0	1	$Q_{n+1} \leftarrow Q_n,\ Q_0 \leftarrow 0$	
SB	1	$[DP, B_1, B_0] \leftarrow 1$	
RB	1	$[DP, B_1, B_0] \leftarrow 0$	
SBT	1/2	Skip if $[DP, B_1, B_0] = 1$	$B_1\ B_0 = 1$
SC	1/2	Skip if $(C) = 1$	$(C) = 1$
SEM	1/2	Skip if $(A_{CC}) = [DP]$	$(A_{CC}) = [DP]$
SEI	1/2	Skip if $(A_{CC}) = I_3\ I_2\ I_1\ I_0$	$(A_{CC}) = I_3\ I_2\ I_1\ I_0$
SK4	1/2	Skip if $K_4 = 1$	$K_4 = 1$
JPT	1	$PC \leftarrow (TR), P_{6-0}$	
JPA	1	$PC_{6-4} \leftarrow P_{6-4}$ $PC_{3-0} \leftarrow P_{3-0} \vee (A_{CC})$	
JCP	1	$PC_{6-0} \leftarrow P_{6-0}$	
CAL	1	$[STACK] \leftarrow (PC)$ $PC \leftarrow 1000\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$	
RT	1	$PC \leftarrow [STACK]$	
RTS	2	$PC \leftarrow [STACK]$ $PC \leftarrow (PC) + 1$	
EIA	1	Enable IA port	
DIA	1	Disable IA port	
EIB	1	Enable IB port	
DIB	1	Disable IB port	
OIU	1	$U_{7-0} \leftarrow I_{7-0}$ $R_{7-0} \leftarrow (Q_{7-0})$	
ERO	1	Enable R port	
DRO	1	Disable R port	
OQR	1	$R \leftarrow (Q)$	
OTR	1	$R_{7-4} \leftarrow (TR),\ R_{3-0} \leftarrow (DP_L)$	
SFS	1	$S \leftarrow (A_{CC})$	
RFS	1	S port Input Mode	
IS	1	$A_{CC} \leftarrow S$	
IK	1	$A_{CC} \leftarrow K$	
RF1	1	$F_1 \leftarrow 0$	
SF1	1	$F_1 \leftarrow 1$	
RF2	1	$F_2 \leftarrow 0$	
SF2	1	$F_2 \leftarrow 1$	
RF3	1	$F_3 \leftarrow 0$	
SF3	1	$F_3 \leftarrow 1$	
RF4	1	$F_4 \leftarrow 0$	
SF4	1	$F_4 \leftarrow 1$	
RF5	1	$F_5 \leftarrow 0$	
SF5	1	$F_5 \leftarrow 1$	
RF6	1	$F_6 \leftarrow 0$	
SF6	1	$F_6 \leftarrow 1$	
RF7	1	$F_7 \leftarrow 0$	
SF7	1	$F_7 \leftarrow 1$	
RF8	1	$F_8 \leftarrow 0$	
SF8	1	$F_8 \leftarrow 1$	
RF9	1	$F_9 \leftarrow 0$	
SF9	1	$F_9 \leftarrow 1$	
RF0	1	$F_0 \leftarrow 0$	
SF0	1	$F_0 \leftarrow 1$	
NOP	1	No Operation	

NEC Microcomputers, Inc.

NEC
μPD548

μCOM-42 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD548 is the only version of the μCOM-42. This PMOS, −10 volt part is designed to have TTL-level compatible inputs and was specifically designed for external RAM expansion. As a μCOM-42, it includes 1920 x 10 ROM, 96 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage V_{GG}	−15 to +0.3 Volts
Input Voltages	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		−2.0	V	
Input Low Voltage	V_{IL}	−4.3		V_{GG}	V	
Output High Voltage	V_{OH1}			−3.0	V	$I_{OH} = -4$ mA ①
Output High Voltage	V_{OH2}			−1.0	V	$I_{OH} = -1$ mA (for S port outputs)
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = -1V$
Input Leakage Current Low	I_{LIL}			−30	μA	$V_I = -36V$
Output Current High	I_{OH}	−1.0			mA	$V_{OH} = -1V$
Output Leakage Current Low	I_{LOL1}			−30	μA	$V_O = -36V$
Output Leakage Current Low	I_{LOL2}			−10	μA	$V_O = -5V$ (for S port outputs)
Supply Current	I_{GG}		−30	−60	mA	

Note: ① For R port, and when only 1 bit is ON (high level)

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$, unless otherwise noted

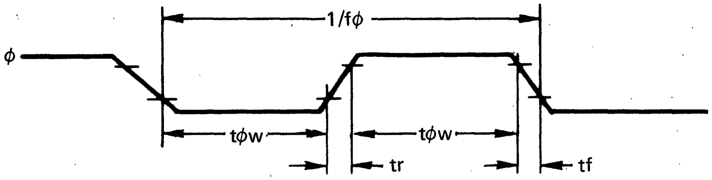
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Frequency	$f\phi$	100		200	KHz	
Clock Pulse Width	$t\phi w$	2.25			μs	
Clock Rise-Fall Time	tr, tf			0.5	μs	

CAPACITANCE

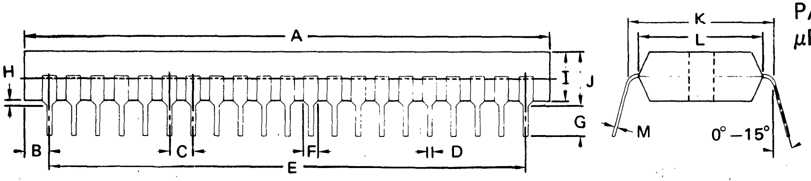
$T_a = 25°C; V_{GG} = -10V \pm 10\%$, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Capacitance, Any Input Except S	C_I			15	pF	f = 1 MHz
Capacitance, Any Output Except S	C_O			15	pF	
S Port Capacitance	C_{IO}			15	pF	

CLOCK WAVEFORM



PACKAGE OUTLINE μPD548C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

NEC Microcomputers, Inc.

NEC
μPD555

EVACHIP-42

DESCRIPTION

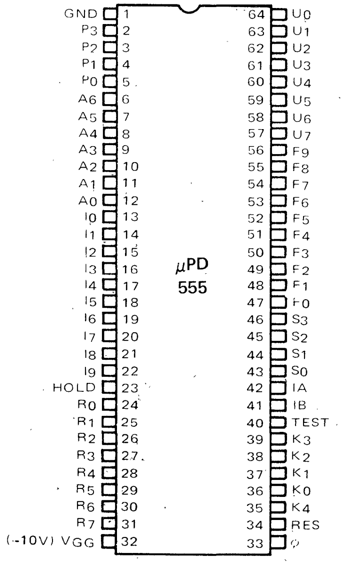
The μPD555 is a system evaluation chip designed to support both hardware and software debugging of the μCOM-42 (μPD548) one-chip microcomputer system.

The μPD555 and the μPD548 have the same functionality in all aspects except that the μPD555 does not contain a read only memory, but provides addressing capability to external memory and HOLD function for step-by-step operation.

FEATURES

- 4-Bit Parallel Processor
- Powerful 72 Instruction Set Including Decimal/Binary Arithmetic Operations
- 10 μs Instruction Cycle Time
- Addressing Capability up to 1920 Words by 10-Bits of External Program Memory
- 96 Words by 4-Bit Data Memory On Chip
- 4-Level Subroutines
- Two Interrupt Input Lines (IA and IB)
- HOLD Capability
- A Variety of Input/Output Ports –
  - – 10 Discrete Output Ports (F_9-F_0)
  - – Two 8-Bit Output Ports (U_7-U_0, R_7-R_0)
  - – 4-Bit Input Port (K_3-K_0)
  - – 4-Bit Input/Output Port (S_3-S_0)
    I/O Level Compatible with μPD5101
  - – 1-Bit Test Input Line
- P-Channel MOS
- Open Drain Output
- Single Power Supply: −10V
- Available in a 64 Pin Ceramic Dual-in-Line Package

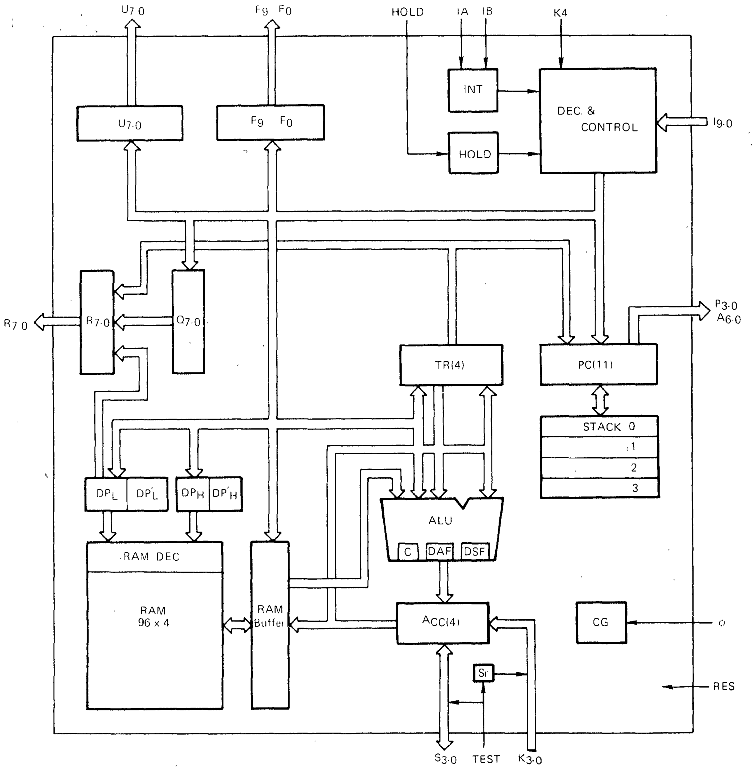
PIN CONFIGURATION



PIN NAMES

$P_0 - P_3$	Page Output
$A_0 - A_6$	Address Output
$I_0 - I_9$	Instruction Input
HOLD	HOLD Input
$R_0 - R_7$	Output Port R
φ	Clock Input
RES	Reset Input
K4	K4 Test Input Line
$K_0 - K_3$	K Input Port
TEST	IC Test Input
IA, IB	Interrupt Input
$S_0 - S_3$	Input/Output Port S
$F_0 - F_9$	Output Port F
$U_0 - U_7$	Output Port U

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	$-10°$C to $+70°$C
Storage Temperature	$-40°$C to $+125°$C
Supply Voltage V_{GG}	-15 to $+0.3$ Volts
All Input Voltages	-20 to $+0.3$ Volts
All Output Voltages	-20 to $+0.3$ Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°$C

CAPACITANCE

$T_a = 25°$C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

DC CHARACTERISTICS

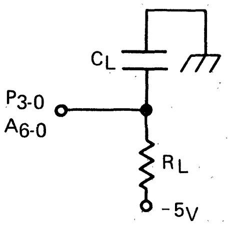
T_a = –10°C to +70°C; V_{GG} = –10V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
High Level Input Voltage	V_{IH}	0		–2.0	V	
Low Level Input Voltage	V_{IL1}	–4.3			V	S, ϕ, $I_{9\text{-}0}$
	V_{IL2}	–7.0			V	Except S, ϕ, $I_{9\text{-}0}$
High Level Input Leakage Current	I_{LIH}			+10	μA	$V_I = -1V$
Low Level Input Leakage Current	I_{LIL}			–10	μA	$V_I = -11V$
High Level Output Current	I_{OH}	–1.0			mA	$V_O = -1V$, except S port
Low Level Output Leakage Current	I_{LOL1}			–30	μA	$V_O = -11V$, except S port
High Level Output Voltage	V_{OH}			–1.75	V	$I_{OH} = -100\,\mu A$, S port
Low Level Output Leakage Current	I_{LOL2}			–10	μA	$V_O = -5V$, S port
Power Supply Current	I_{GG}		–30	–60	mA	

AC CHARACTERISTICS

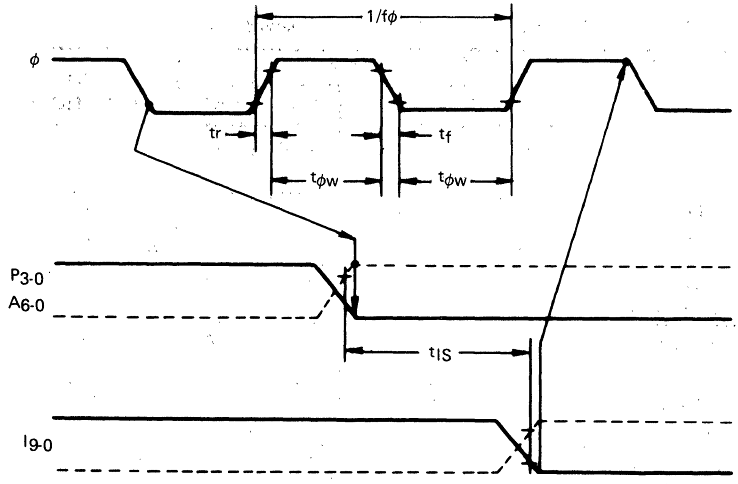
T_a = –10°C to +70°C, V_{GG} = –10V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Frequency	f_ϕ	100		200	KHz	
Clock Pulse Width	$t_{\phi W}$	2.25				
Clock Rise and Fall Times	tr, tf			0.5	μs	
Input Setup Time from Output	t_{IS}			2.5	μs	C_L = 100 pF, R_L = 5.1 KΩ

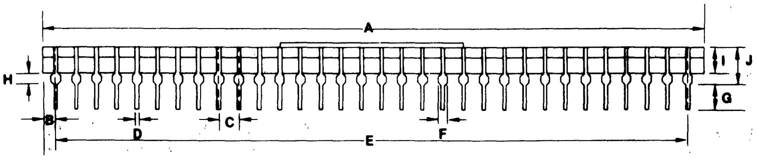


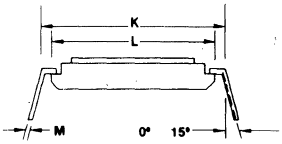
LOAD CIRCUIT

TIMING WAVEFORM



PACKAGE OUTLINE μPD555D





ITEM	MILLIMETERS	INCHES
A	82.0 MAX	3.23 MAX
B	1.6	0.063
C	2.54	0.1
D	0.43 ± 0.1	0.017 ± 0.004
E	78.8	3.1
F	1.27	0.05
G	3.2 MIN	0.13 MIN
H	1.3 MIN	0.05 MIN
I	3.9	0.154
J	5.2 MAX	0.205 MAX
K	22.96	0.904
L	20.3	0.8
M	0.3 ± 0.1	0.012 ± 0.004

NEC

NEC Microcomputers, Inc.

μCOM-43/44/45 4-BIT SINGLE CHIP MICROCOMPUTERS

DESCRIPTION

The μCOM-43 Family consists of three device types designed to offer a full range of cost/performance tradeoffs. All three devices share compatible hardware and instruction set. The μCOM-43 Family is designed for general purpose controller applications and offers ideal devices for industrial controls, appliance controls, games, etc.

All three devices contain the functional blocks necessary to enable their use for both industrial and non-industrial controller applications. These blocks include: a 4-bit parallel ALU; 8-bit wide ROM for program storage; 4-bit wide RAM for data storage; stack register for subroutines; extensive I/O; and an on-chip clock generator.

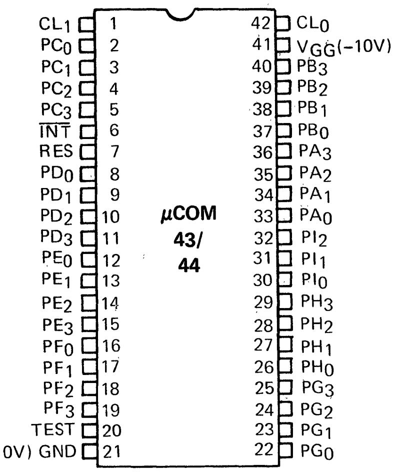
The instruction set of the μCOM-43 Family is designed to perform controller-oriented functions and for efficient use of the fixed program memory space. The instruction set includes a number of multifunction instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

The three device types comprising the μCOM-43 Family are differentiated by ROM/RAM size and I/O lines. The μCOM-43 has 2000 x 8 ROM, 96 x 4 RAM and 35 I/O lines. The μCOM-44 has 1000 x 8 ROM, 64 x 4 RAM and 35 I/O lines. The μCOM-45 has 1000 x 8 or 640 x 8 ROM, 32 x 4 RAM and 21 I/O lines. In addition, the μCOM-43 has real hardware interrupt, 3 level stack and programmable timer, while the μCOM-44/45 have pseudo-interrupt capability and a single level stack.

FEATURES

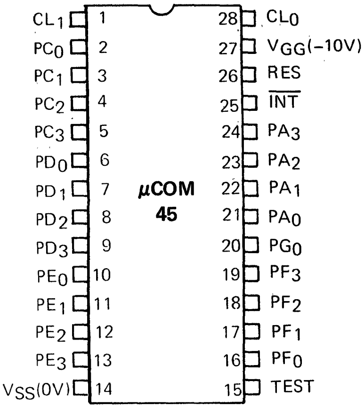
- Stand Alone 4-Bit Microcomputers for Control Applications
- Powerful Instruction Set Capable of: Binary Addition; Decimal Addition and Subtraction; Logical Operations
- 10 μs Instruction Cycle
- Choice of ROM Size: 2000 x 8 – μCOM-43
  1000 x 8 – μCOM-44
  1000 x 8 – μCOM-45
  640 x 8
- Choice of RAM Size: 96 x 4 – μCOM-43
  64 x 4 – μCOM-44
  32 x 4 – μCOM-45
- Choice of I/O Power: 35 lines – μCOM-43
  35 lines – μCOM-44
  21 lines – μCOM-45
- All Capable of Single Bit Manipulation and 4-Bit Parallel Processing.
- Interrupt Capability
- On-Chip Clock Generator
- Open Drain Outputs
- Choice of PMOS or CMOS Technology, Both Requiring Single Supplies
- Available in 42 Pin or 28 Pin Plastic Dual-in-Line Packages

PIN CONFIGURATIONS



PIN NAMES

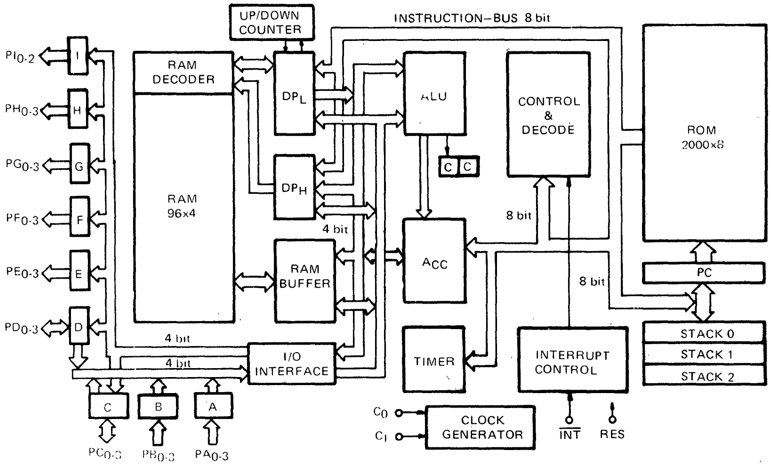
CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
TEST	Input for Testing (Normally GND)
PG_0–PG_3	Output Port G
PH_0–PH_3	Output Port H
PI_0–PI_3	Output Port I
PA_0–PA_3	Input Port A
PB_0–PB_3	Input Port B



PIN NAMES

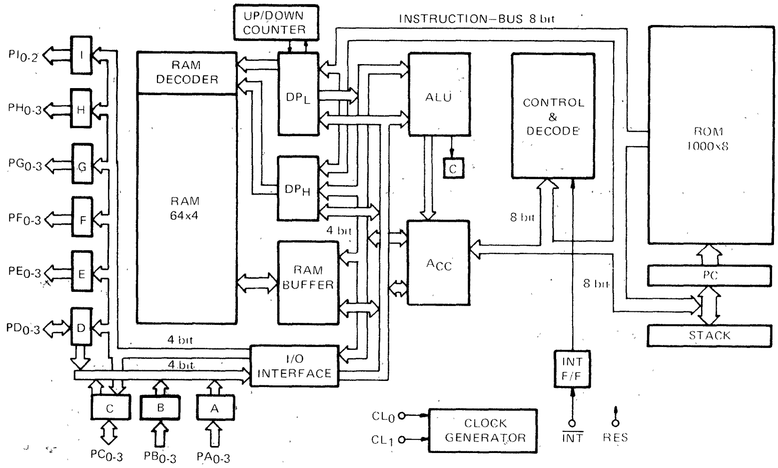
CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
PG_0	Output Port G
PA_0–PA_3	Input Port A
$\overline{INT}$	Interrupt Input
RES	Reset

BLOCK DIAGRAM
μCOM-43

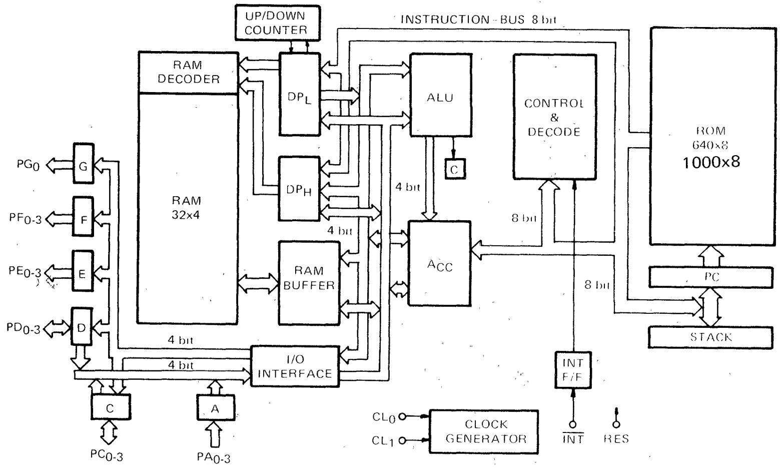


BLOCK DIAGRAMS

μCOM-44



μCOM-45



FUNCTIONAL DESCRIPTION

Program Counter

The 11-bit program counter (10-bit for μCOM-44/45) is organized as a 3-bit register (2-bit for μCOM-44/45) and an 8-bit binary up-counter (lower eight bits). The contents of the upper register specify one of the fields of the ROM. The 8-bit binary counter is divided so that the contents of the higher two bits specify one of four pages in a field and the lower six bits specify one of 64 addresses in a page. The contents of the lower eight bits of the program counter (8-bit binary up-counter) are simply incremented to execute the instructions sequentially. In a field, a page is automatically extended to the next one and four pages (256 bytes) are automatically executed.

Stack Register

The stack register is a last-in-first-out (LIFO) push down stack register organized as 3 words x 11 bits (1 word x 10 bits for μCOM-44/45). This register is used to save the contents of the program counter (return address) when a subroutine is called or an interrupt is acknowledged.

ROM (Read-Only Memory)

The user's application program is stored in the 8-bit wide mask programmable read-only memory (ROM). The ROM is organized into fields and pages. The 2000 word ROM of the μCOM-43 has eight fields, the 1000 word ROM of the μCOM-44/45 has four fields and the 640 word ROM of the low-end μCOM-45 has two fields. Each field is divided into four pages of 64 words each, and each word consists of eight bits.

RAM (Data Memory)

The RAM is organized in a multi-row by 16 column configuration. It is addressed by a data pointer of which the higher bits (DPH) address the row and the lower bits (DPL) address the column. The exact RAM size for each device is shown below.

	RAM	ROW/COLUMN ORGANIZATION	DPH	DPL
μCOM-43	96 x 4	6 x 16	3	4
μCOM-44	64 x 4	4 x 16	2	4
μCOM-45	32 x 4	2 x 16	1	4

Internal Registers

The ALU (Arithmetic Logic Unit) and the ACC (Accumulator) form the heart of the μCOM-43 Family microcomputer system. The ALU performs arithmetic and logical operations and tests for operation results. The result of an operation by the ALU is stored in the ACC and in the carry F/F. The ACC is a 4-bit register which stores ALU results and other data to be processed. The carry F/F is a single bit flip-flop which indicates when a carry bit is generated during addition.

Flag Register (μCOM-43 Only)

A 4-bit word in the RAM can be specifically used as a software controlled general purpose flag register. The individual flag bits can be set or reset and tested for either a 1 or a 0. This can be done directly without modifying the RAM data pointer.

Working Registers (μCOM-43 Only)

There are six words in RAM that can be used as 4-bit general purpose working registers. These registers can be directly manipulated without modification of the data pointer and are used for data transfer and exchange between the data pointer and the working register, and between the ACC and the working register.

Programmable Interval Timer (μCOM-43 Only)

The μCOM-43 contains a software programmable interval timer composed of a 6-bit polynomial counter and a 6-bit programmable binary counter.

The initial setting of the timer is done using the timer set instruction STM, with the timer starting to count at the end of the STM instruction execution. The STM instruction contains six binary bits of immediate data which is loaded in the 6-bit programmable binary counter upon STM instruction execution. By varying the 6-bit immediate data, one of 64 time intervals can be programmed.

I/O Ports

The μCOM-43/44 have 35 input/output ports (μCOM-45 has 21) for communication with and control of the external world. These ports are organized into nine input/output ports (A to I). Eight ports (A to H) are composed of four bits each and the last port (I) is composed of three bits.

Input Ports	(4 bits each): A, B ①
Input/Output Ports	(4 bits each): C, D
Output Ports	(4 bits each): E, F, G ②, H ①
Output Ports	(3 bits): I ①

Notes: ① Not on μCOM-45.

② G Port on μCOM-45 is a single line.

FUNCTIONAL DESCRIPTION (CONT.)

In order to provide flexible and efficient use of these I/O ports, a variety of input/output instructions are provided which enable single bit set/reset, single bit test and conditional skip, 4-bit parallel input/output and 8-bit immediate parallel output. The I/O instructions are divided into two types, the ones dedicated to specific ports and the ones that use the 4-bit data in the DPL to select a desired port. The former include such instructions as IA and OE that specifically access port A and E, respectively. The latter require that a 4-bit code assigned to the desired port be loaded into the DPL using data pointer manipulation instructions prior to I/O instruction execution.

INSTRUCTION SET

The μCOM-43 has an 80 instruction set. The μCOM-44/45 have a 58 instruction subset of the μCOM-43. The majority of the 22 instruction difference is related to added hardware features of the μCOM-43. The instruction set is summarized below.

MNEMONIC	BYTES	CYCLES	DESCRIPTION	CONDITION FOR SKIP
CLA	1	1	$A_{CC} \leftarrow 0$	
CMA	1	1	$A_{CC} \leftarrow (\overline{A_{CC}})$	
CIA	1	1	$A_{CC} \leftarrow (\overline{A_{CC}})+1$	
INC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+1$; skip if Carry	Carry
DEC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})-1$; skip if Borrow	Borrow
CLC	1	1	$C \leftarrow 0$	
STC	1	1	$C \leftarrow 1$	
XC	1	1	$(C) \leftrightarrows (C')$	
RAR	1	1	$(A_{CCn-1}) \leftarrow (A_{CCn})$, $C \leftarrow (A_{CC0})$, $(A_{CC3}) \leftarrow (C)$	
INM	1	1/2-3	$[(DP)] \leftarrow [(DP)]+1$; skip if $[(DP)]=0$	$[(DP)]=0$
DEM	1	1/2-3	$[(DP)] \leftarrow [(DP)]-1$; skip if $[(DP)]=F$	$[(DP)]=F$
AD	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+[(DP)]$; skip if Carry	Carry
ADS	1	1/2-3	$A_{CC}, C \leftarrow (A_{CC})+[(DP)]+(C)$; skip if Carry	Carry
ADC	1	1	$A_{CC}, C \leftarrow (A_{CC})+[(DP)]+(C)$	
DAA	1	1	$A_{CC} \leftarrow (A_{CC})+6$	
DAS	1	1	$A_{CC} \leftarrow (A_{CC})+10$	
EXL	1	1	$A_{CC} \leftarrow (A_{CC}) \forall [(DP)]$	
LI	1	1	$A_{CC} \leftarrow I_3 I_2 I_1 I_0$	
S	1	1	$[(DP)] \leftarrow (A_{CC})$	
L	1	1	$A_{CC} \leftarrow [(DP)]$	
LM	1	1	$A_{CC} \leftarrow [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$	
X	1	1	$(A_{CC}) \leftrightarrows [(DP)]$	
XM	1	1	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$	
XD	1	1/2-3	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
XMD	1	1/2-3	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$; $DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
XI	1	1/2-3	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
XMI	1	1/2-3	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$; $DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
LDI	2	2	$DP \leftarrow I_6 - I_0$	
LDZ	1	1	$DP_H \leftarrow 0$; $DP_L \leftarrow I_3 I_2 I_1 I_0$	
DED	1	1/2-3	$DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
IND	1	1/2-3	$DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
TAL	1	1	$DP_L \leftarrow (A_{CC})$	
TLA	1	1	$A_{CC} \leftarrow (DP_L)$	

MNEMONIC	BYTES	CYCLES	DESCRIPTION	CONDITION FOR SKIP
XHX	1	2	$(X)\leftrightarrow(DP_H)$	
XLY	1	2	$(Y)\leftrightarrow(DP_L)$	
THX	1	2	$X\leftarrow(DP_H)$	
TLY	1	2	$Y\leftarrow(DP_L)$	
XAZ	1	2	$(Z)\leftrightarrow(A_{CC})$	
XAW	1	2	$(W)\leftrightarrow(A_{CC})$	
TAZ	1	2	$Z\leftarrow(A_{CC})$	
TAW	1	2	$W\leftarrow(A_{CC})$	
XHR	1	2	$(R)\leftrightarrow(DP_H)$	
XLS	1	2	$(S)\leftrightarrow(DP_L)$	
SMB	1	1	$[(DP, B_1B_0)]\leftarrow1$	
RMB	1	1	$[(DP, B_1B_0)]\leftarrow0$	
TMB	1	1/2-3	skip if $[(DP, B_1B_0)]=1$	$[(DP, B_1B_0)]=1$
TAB	1	1/2-3	skip if $(A_{CC}(B_1B_0))=1$	$(A_{CC}(B_1B_0))=1$
CMB	1	1/2-3	skip if $(A_{CC}(B_1B_0))=[(DP, B_1B_0)]$	$(A_{CC}(B_1B_0))=[(DP, B_1B_0)]$
SFB	1	2	FLAG $(B_1B_0)\leftarrow1$	
RFB	1	2	FLAG $(B_1B_0)\leftarrow0$	
FBT	1	2/3-4	skip if (FLAG $(B_1B_0))=1$	(FLAG$(B_1B_0))=1$
FBF	1	2/3-4	skip if (FLAG $(B_1B_0))=0$	(FLAG$(B_1B_0))=0$
CM	1	1/2-3	skip if $(A_{CC})=[(DP)]$	$(A_{CC})=[(DP)]$
CI	2	2/3-4	skip if $(A_{CC})=I_3I_2I_1I_0$	$(A_{CC})=I_3I_2I_1I_0$
CLI	2	2/3-4	skip if $(DP_L)=I_3I_2I_1I_0$	$(DP_L)=I_3I_2I_1I_0$
TC	1	1/2-3	skip if $(C)=1$	$(C)=1$
TIT	1	1/2-3	skip if (INT F/F)=1; INT F/F←0	(INT F/F)=1
JCP	1	1	$PC_{5-0}\leftarrow P_5\text{-}P_0$	
JMP	2	2	$PC\leftarrow P_{10}\text{-}P_0$	
JPA	1	2	$PC_{5-0}\leftarrow A_3A_2A_1A_000$	
EI	1	1	INTE F F←1	
DI	1	1	INTE F F←0	
CZP	1	1	STACK←(PC) $PC\leftarrow00000P_3P_2P_1P_000$	
CAL	2	2	STACK←(PC); $PC\leftarrow P_{10}\text{-}P_0$	
RT	1	2	PC←(STACK)	
RTS	1	3-4	PC←(STACK); PC←(PC)+1,2	Unconditional
STM	2	2	TM F F←0; TIMER$\leftarrow I_5\text{-}I_0$	
TTM	1	1/2-3	skip if (TM F/F)=1	(TM F/F)=1
SEB	1	2	PORT E $(B_1B_0)\leftarrow1$	
REB	1	1	PORT E $(B_1B_0)\leftarrow0$	
SPB	1	1	PORT $(DP_L, B_1B_0)\leftarrow1$	
RPB	1	1	PORT $(DP_L, B_1B_0)\leftarrow0$	
TPA	1	2/3-4	skip if (PORT A $(B_1B_0))=1$	(PORT A $(B_1B_0))=1$
TPB	1	1/2-3	skip if (PORT $(DL_L, B_1B_0))=1$	(PORT $(DP_L, B_1B_0)=1$
OE	1	2	PORT E$\leftarrow(A_{CC})$	
OP	1	1	PORT $(DP_L)\leftarrow(A_{CC})$	
OCD	2	2	PORT C,D$\leftarrow I_7\text{-}I_0$	
IA	2	2	$A_{CC}\leftarrow$(PORT A)	
IP	1	1	$A_{CC}\leftarrow$(PORT (DP_L))	
NOP	1	1	No Operation	

▨ These instructions apply only to the µCOM-43.

NEC Microcomputers, Inc.

NEC
μPD546

μCOM-43 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD546 is the standard version of the μCOM-43. This PMOS, –10 volt part is designed to have TTL-level compatible inputs and is easily interfaced to external static RAM. As a μCOM-43, it includes 2000 x 8 ROM, 96 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	–10°C to +70°C
Storage Temperature	–40°C to +125°C
Supply Voltage	–15 to +0.3 Volts
Input Voltages	–15 to +0.3 Volts
Output Voltages	–15 to +0.3 Volts
Output Current	–4 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC/AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -10V \pm 10\%$

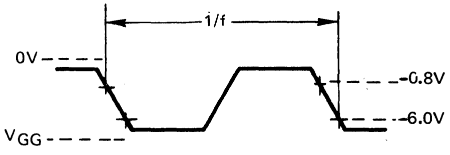
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		-2.0	V	Ports A to D, $\overline{\text{INT}}$, RES
Input Low Voltage	V_{IL}	-4.3		V_{GG}	V	Ports A to D, $\overline{\text{INT}}$, RES
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, $\overline{\text{INT}}$, RES, TEST $V_I = -1V$
Input Leakage Current Low	I_{LIL}			-10	μA	Ports A and B, $\overline{\text{INT}}$, RES, TEST $V_I = -11V$
I/O Leakage Current High	I_{IOH}			+30	μA	Ports C and D $V_I = -1V$
I/O Leakage Current Low	I_{IOL}			-30	μA	Ports C and D $V_I = -11V$
Output Voltage	V_{OH1}			-1.0	V	Ports C to I $I_{OH} = -1.0$ mA
	V_{OH2}			-2.3	V	Ports C to I $I_{OH} = -3.3$ mA
Output Leakage Current	I_{OL}			-10	μA	Ports C to I $V_O = -11V$
Supply Current	I_{GG}		-30	-50	mA	
Oscillator Frequency	F	150		440	KHz	

CAPACITANCE

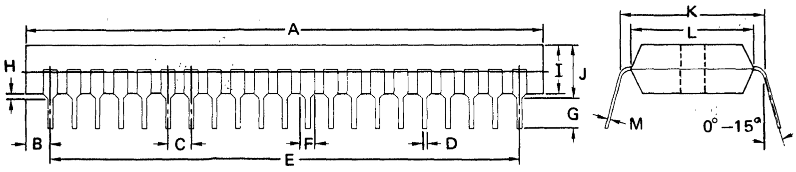
$T_a = 25°C$, f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE
μPD546C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

NEC Microcomputers, Inc.

NEC
μPD547

μCOM-44 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD547 is the standard version of the μCOM-44. This PMOS, −10 volt part is designed to have TTL-level compatible inputs and is easily interfaced to external static RAM. As a μCOM-44, it includes 1000 x 8 ROM, 64 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages	−15 to +0.3 Volts
Output Voltages	−15 to +0.3 Volts
Output Current	−4 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

$^*T_a = 25°C$

DC/AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -10V \pm 10\%$

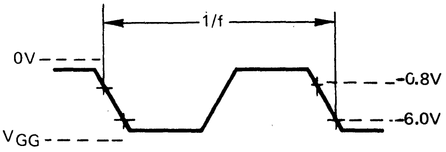
		LIMITS				
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		−2.0	V	Ports A to D, $\overline{INT}$, RES
Input Low Voltage	V_{IL}	−4.3		V_{GG}	V	Ports A to D, $\overline{INT}$, RES
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, $\overline{INT}$, RES, TEST $V_I = -1V$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A and B, $\overline{INT}$, RES, TEST $V_I = -11V$
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D $V_I = -1V$
I/O Leakage Current Low	I_{IOL}			−10	μA	Ports C and D $V_I = -11V$
Output Voltage	V_{OH1}			−1.0	V	Ports C to I $I_{OH} = -1.0$ mA
	V_{OH2}			−2.3	V	Ports C to I $I_{OH} = -3.3$ mA
Output Leakage Current	I_{OL}			−10	μA	Ports C to I $V_O = -11V$
Supply Current	I_{GG}		−30	−50	mA	
Oscillator Frequency	F	150		440	KHz	

CAPACITANCE

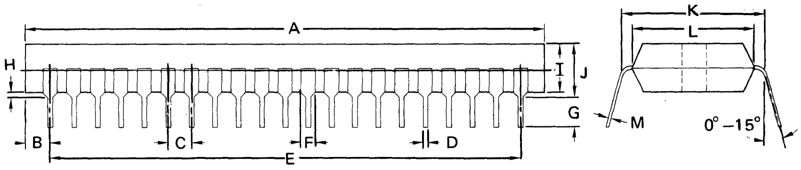
$T_a = 25^\circ C$, f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE μPD547C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

NEC Microcomputers, Inc.

NEC
μPD547L

μCOM-44 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD547L is a low power version of the μCOM-44. It is a modified PMOS device requiring a −8 volt power supply with a reduced supply current specification. As a μCOM-44, it includes 1000 x 8 ROM, 64 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages	−15 to +0.3 Volts
Output Voltages	−15 to +0.3 Volts
Output Current	−4 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC/AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -8V \pm 10\%$

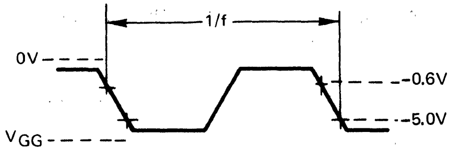
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	0		−1.6	V	Ports A to D, $\overline{\text{INT}}$, RES
Input Low Voltage	V_{IL}	−3.8		V_{GG}	V	Ports A to D, $\overline{\text{INT}}$, RES
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, $\overline{\text{INT}}$, RES, TEST $V_I = -1V$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A and B, $\overline{\text{INT}}$, RES, TEST $V_I = -9V$
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D $V_I = -1V$
I/O Leakage Current Low	I_{IOL}			−10	μA	Ports C and D $V_I = -9V$
Output Voltage	V_{OH1}			−1.0	V	Ports C to I $I_{OH} = -0.7$ mA
	V_{OH2}			−2.3	V	Ports C to I $I_{OH} = -2.6$ mA
Output Leakage Current	I_{OL}			−10	μA	Ports C to I $V_O = -9V$
Supply Current	I_{GG}		−15	−25	mA	
Oscillator Frequency	F	100		180	KHz	

CAPACITANCE

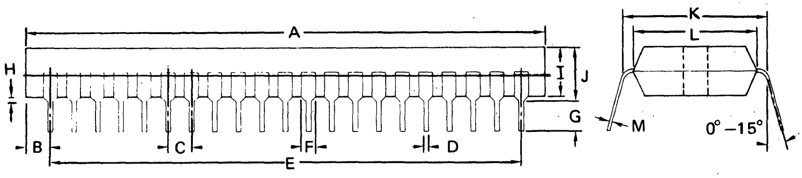
$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE μPD547LC



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

NEC Microcomputers, Inc.

NEC
µPD550

µCOM-45 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The µPD550 is the 640 x 8 ROM version of the µCOM-45. This PMOS, −10 volt part features both TTL-level compatible inputs as well as outputs capable of being pulled to −35 volts. This allows direct interfacing with Fluorescent Indicator Panels (FIPs). As a µCOM-45, it includes 32 x 4 RAM and 21 I/O lines in a 28 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages (Port A, $\overline{\text{INT}}$, RES, TEST)	−15 to +0.3 Volts
(All Other Inputs)	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts
Output Current (Ports C, D)	−4 mA
(Ports E, F, G)	−15 mA
(Total Current)	−60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C.

DC/AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −10V ± 10%.

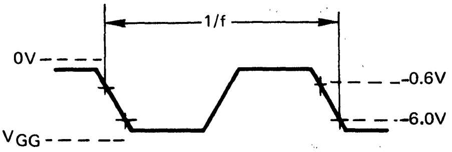
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	0		−2.0	V	Ports A, C, D, $\overline{\text{INT}}$, RES
Input Low Voltage	V_{IL1}	−4.3		V_{GG}	V	Ports A, $\overline{\text{INT}}$, RES
	V_{IL2}	−4.3		−35	V	Port C and D
Input Leakage Current High	I_{LIH}			+10	µA	Ports A, $\overline{\text{INT}}$, RES, TEST V_I = 1V
Input Leakage Current Low	I_{LIL1}			−10	µA	Ports A, $\overline{\text{INT}}$, RES, TEST V_I = −11V
	I_{LIL2}			−30	µA	Port A V_I = −35V
I/O Leakage Current High	I_{IOH}			+10	µA	Ports C and D V_I = −1V
I/O Leakage Current Low	I_{IOL1}			−10	µA	Ports C and D V_I = −11V
	I_{IOL2}			−30	µA	Ports C and D V_I = −35V
Output Voltage	V_{OH1}			−1.0	V	Ports C and D I_O = −2 mA
	V_{OH2}			−2.5	V	Ports E, F, G I_O = −10 mA
Output Leakage Current	I_{OL1}			−10	µA	Ports C, D, E, F, G V_O = −11V
	I_{OL2}			−30	µA	Ports C, D, E, F, G V_O = −35V
Supply Current	I_{GG}		−20	−40	mA	
Oscillator Frequency	F	150		440	KHz	

CAPACITANCE

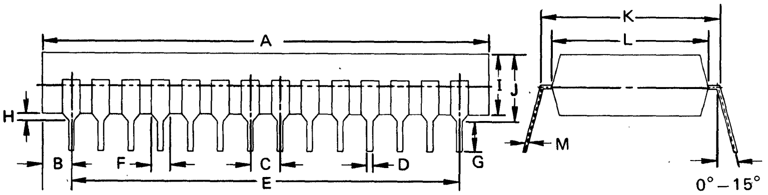
$T_a = 25^\circ C$, f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE
μPD550C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{\ 0.05}$	$0.01^{+0.004}_{\ 0.002}$

NEC Microcomputers, Inc.

NEC
μPD552

μCOM-44 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD552 is a high negative output version of the μCOM-44. This PMOS, -10 volt part is designed with outputs capable of being pulled to -35 volts. This allows direct interfacing with Fluorescent Indicator Panels (FIPs). As a μCOM-44, it includes 1000 x 8 ROM, 64 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-15 to +0.3 Volts
Input Voltages (Port A, $\overline{\text{INT}}$, RES, TEST)	-15 to +0.3 Volts
(All Other Inputs)	-40 to +0.3 Volts
Output Voltages	-40 to +0.3 Volts
Output Current (Each Output Bit)	-12 mA
(Total Current)	-60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC/AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -10V \pm 10\%$

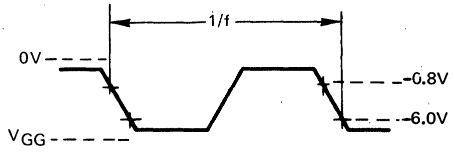
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		-3.5	V	Ports A to D, $\overline{\text{INT}}$, RES
Input Low Voltage	V_{IL1}	-7.5		V_{GG}	V	Ports A and B, $\overline{\text{INT}}$, RES
	V_{IL2}	-7.5		-35	V	Ports C and D
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, $\overline{\text{INT}}$, RES, TEST $V_I = -1V$
Input Leakage Current Low	I_{LIL1}			-10	μA	Ports A and B, $\overline{\text{INT}}$, RES, TEST $V_I = -11V$
	I_{LIL2}			-30	μA	Ports A and B $V_I = -35V$
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D $V_I = -1V$
I/O Leakage Current Low	I_{IOL1}			-10	μA	Ports C and D $V_I = -11V$
	I_{IOL2}			-30	μA	Ports C and D $V_I = -35V$
Output Voltage	V_{OH}			-2.0	V	Ports C to I $I_O = -8$ mA
Output Leakage Current	I_{OL1}			-10	μA	Ports C to I $V_O = -11V$
	I_{OL2}			-30	μA	Ports C to I $V_O = -35V$
Supply Current	I_{GG}		-30	-50	mA	
Oscillator Frequency	F	150		440	KHz	

CAPACITANCE

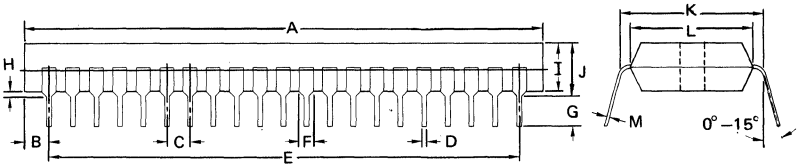
$T_a = 25^\circ C$, f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE μPD552C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

NEC

NEC Microcomputers, Inc.

μPD553

μCOM-43 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD553 is a high negative output version of the μCOM-43. This PMOS, −10 volt part is designed with outputs capable of being pulled to −35 volts. This allows direct interfacing with Fluorescent Indicator Panels (FIPs). As a μCOM-43, it includes 2000 x 8 ROM, 96 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages (Port A, $\overline{\text{INT}}$, RES, TEST)	−15 to +0.3 Volts
(All Other Inputs)	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts
Output Current (Each Output Bit)	−12 mA
(Total Current)	−60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC/AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -10V \pm 10\%$

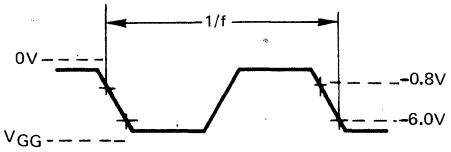
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		−3.5	V	Ports A to D, $\overline{\text{INT}}$, RES
Input Low Voltage	V_{IL1}	−7.5		V_{GG}	V	Ports A and B, $\overline{\text{INT}}$, RES
	V_{IL2}	−7.5		−35	V	Ports C and D
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, $\overline{\text{INT}}$, RES, TEST $V_I = -1V$
Input Leakage Current Low	I_{LIL1}			−10	μA	Ports A and B, $\overline{\text{INT}}$, RES, TEST $V_I = -11V$
	I_{LIL2}			−30	μA	Ports A and B $V_I = -35V$
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D $V_I = -1V$
I/O Leakage Current Low	I_{IOL1}			−10	μA	Ports C and D $V_I = -11V$
	I_{IOL2}			−30	μA	Ports C and D $V_I = -35V$
Output Voltage	V_{OH}			−2.0	V	Ports C to I $I_O = -8$ mA
Output Leakage Current	I_{OL1}			−10	μA	Ports C to I $V_O = -11V$
	I_{OL2}			−30	μA	Ports C to I $V_O = -35V$
Supply Current	I_{GG}		−30	−50	mA	
Oscillator Frequency	F	150		440	KHz	

CAPACITANCE

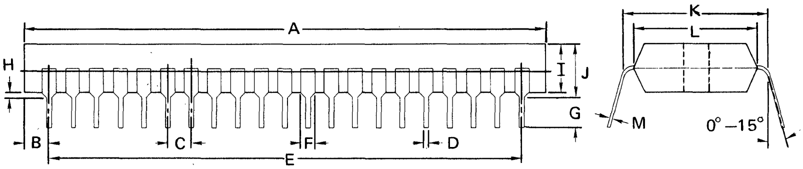
$T_a = 25°C$, f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE μPD553C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

NEC Microcomputers, Inc.

NEC
μPD554

μCOM-45 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD554 is the 1000 x 8 ROM version of the μCOM-45. This PMOS, -10 volt part features both TTL-level compatible inputs as well as outputs capable of being pulled to -35 volts. This allows direct interfacing with Fluorescent Indicator Panels (FIPs). As a μCOM-45, it includes 32 x 4 RAM and 21 I/O lines in a 28 pin plastic, dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-15 to +0.3 Volts
Input Voltages (Port A, $\overline{\text{INT}}$, RES, TEST)	-15 to +0.3 Volts
(All Other Inputs)	-40 to +0.3 Volts
Output Voltages	-40 to +0.3 Volts
Output Current (Ports C, D)	-4 mA
(Ports E, F, G)	-15 mA
(Total Current)	-60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC/AC CHARACTERISTICS

T_a = -10°C to +70°C, V_{GG} = -10V ± 10%.

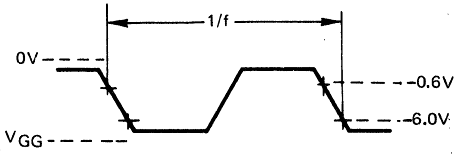
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	0		-2.0	V	Ports A, C, D, $\overline{\text{INT}}$, RES
Input Low Voltage	V_{IL1}	-4.3		V_{GG}	V	Ports A, $\overline{\text{INT}}$, RES
	V_{IL2}	-4.3		-35	V	Port C and D
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, $\overline{\text{INT}}$, RES, TEST V_I = 1V
Input Leakage Current Low	I_{LIL1}			-10	μA	Ports A, $\overline{\text{INT}}$, RES TEST V_I = -11V
	I_{LIL2}			-30	μA	Port A V_I = -35V
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D V_I = -1V
I/O Leakage Current Low	I_{IOL1}			-10	μA	Ports C and D V_I = -11V
	I_{IOL2}			-30	μA	Ports C and D V_I = -35V
Output Voltage	V_{OH1}			-1.0	V	Ports C and D I_O = -2 mA
	V_{OH2}			-2.5	V	Ports E, F, G I_O = -10 mA
Output Leakage Current	I_{OL1}			-10	μA	Ports C, D, E, F, G V_O = -11V
	I_{OL2}			-30	μA	Ports C, D, E, F, G V_O = -35V
Supply Current	I_{GG}		-20	-40	mA	
Oscillator Frequency	F	150		440	KHz	

CAPACITANCE

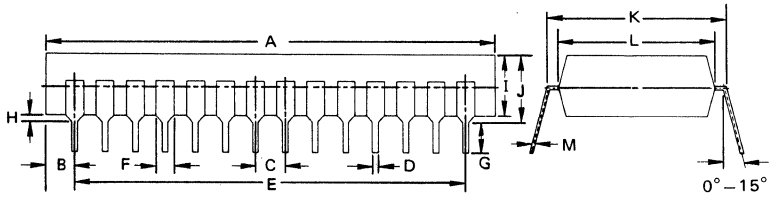
$T_a = 25°C$, f = 1 MHz.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE μPD554C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

NEC Microcomputers, Inc.

NEC
μPD650

μCOM-43 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD650 is a CMOS version of the μCOM-43. It features a single +5 volt power supply, a 2 mA (max), 800 μA (typ) current drain and extended temperature range. As a μCOM-43, it includes 2000 x 8 ROM, 96 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-30°C to +85°C
Storage Temperature	-55°C to +125°C
Supply Voltage	-0.3 to +7.0 Volts
Input Voltages	-0.3 to +7.0 Volts
Output Voltages	-0.3 to +7.0 Volts
Output Current (Each Output Bit)	2.5 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC/AC CHARACTERISTICS

$T_a = -30°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$.

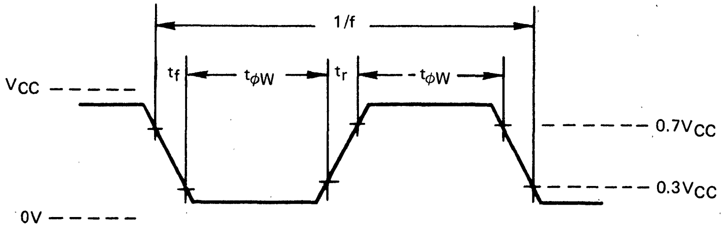
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	$0.7V_{CC}$		V_{CC}	V	Ports A to D, $\overline{INT}$, RES
Input Low Voltage	V_{IL}	0		$0.3V_{CC}$	V	Ports A to D, $\overline{INT}$, RES
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, $\overline{INT}$, RES ($V_I = V_{CC}$)
Input Leakage Current Low	I_{LIL}			-10	μA	Ports A and B, $\overline{INT}$, RES ($V_I = 0V$)
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D ($V_I = V_{CC}$)
I/O Leakage Current Low	I_{IOL}			-10	μA	Ports C and D ($V_0 = 0_V$)
Output High Voltage 1	V_{OH1}	V_{CC}-0.5			V	Ports C and D ($I_{OH} = -1$ mA)
		V_{CC}-0.5			V	Ports E and I ($I_{OH} = -0.6$ mA)
Output High Voltage 2	V_{OH2}	V_{CC}-2.5			V	Ports C to I ($I_{OH} = -2$ mA)
Output Low Voltage	V_{OL1}			0.6	V	Ports E to I ($I_{OL} = 2$ mA)
	V_{OL2}			0.4	V	Ports E to I ($I_{OL} = 7.2$ mA)
Supply Current	I_{CC}		0.8	2.0	mA	
Clock High Voltage	$V_{\phi H}$	$0.7V_{CC}$		V_{CC}	V	CLO, Ext. Clk.
Clock Low Voltage	$V_{\phi L}$	0		$0.3V_{CC}$	V	CLO, Ext. Clk.
Clock Leakage Current High	$I_{L\phi H}$			200	μA	CLO, Ext. Clk. ($V_{OH} = V_{CC}$)
Clock Leakage Current Low	$I_{L\phi L}$			-200	μA	CLO, Ext. Clk. ($V_{OL} = 0V$)
Clock Frequency	f	150		440	KHz	
Clock Rise and Fall Times	tr, tf	0		0.3	μs	Ext. Clk.
Clock Pulse Width	$t_{\phi W}$	0.5		5.6	μs	Ext. Clk.

CAPACITANCE

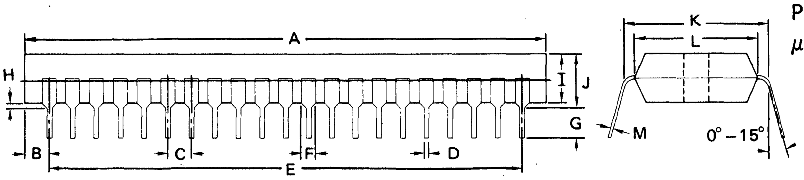
T_a = −30°C to +85°C, V_{CC} = +5V ± 10%.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
I/O Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE μPD650C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

SP650-9-78-GN-CAT

NEC Microcomputers, Inc.

NEC
μPD651

μCOM-44 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD651 is a CMOS version of the μCOM-44. It features a single +5 volt power supply, a 2 mA (max), 800 μA (typ) current drain and extended temperature range. As a μCOM-44, it includes 1000 x 8 ROM, 64 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−30°C to +85°C
Storage Temperature	−55°C to +125°C
Supply Voltage	−0.3 to +7.0 Volts
Input Voltages	−0.3 to +7.0 Volts
Output Voltages	−0.3 to +7.0 Volts
Output Current (Each Output Bit)	2.5 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

*$T_a = 25°C$

DC/AC CHARACTERISTICS

$T_a = -30°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$.

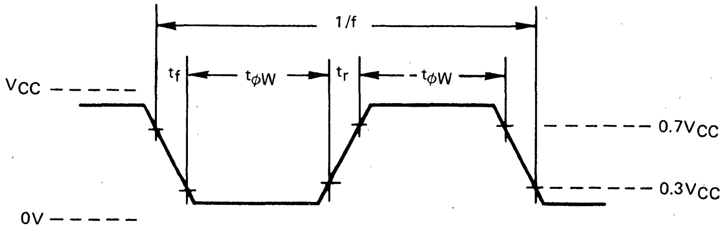
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	$0.7V_{CC}$		V_{CC}	V	Ports A to D, $\overline{INT}$, RES
Input Low Voltage	V_{IL}	0		$0.3V_{CC}$	V	Ports A to D, $\overline{INT}$, RES
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, $\overline{INT}$, RES ($V_I = V_{CC}$)
Input Leakage Current Low	I_{LIL}			-10	μA	Ports A and B, $\overline{INT}$, RES ($V_I = 0V$)
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D ($V_I = V_{CC}$)
I/O Leakage Current Low	I_{IOL}			-10	μA	Ports C and D ($V_O = 0_V$)
Output High Voltage 1	V_{OH1}	V_{CC}-0.5			V	Ports C and D ($I_{OH} = -1$ mA)
		V_{CC}-0.5			V	Ports E to I ($I_{OH} = -1$ mA)
Output High Voltage 2	V_{OH2}	V_{CC}-2.5			V	Ports C to I ($I_{OH} = -2$ mA)
Output Low Voltage	V_{OL1}			0.6	V	Ports E to I ($I_{OL} = 2$ mA)
	V_{OL2}			0.4	V	Ports E to I ($I_{OL} = 1.2$ mA)
Supply Current	I_{CC}		0.8	2.0	mA	
Clock High Voltage	$V_{\phi H}$	$0.7V_{CC}$		V_{CC}	V	CLO, Ext. Clk.
Clock Low Voltage	$V_{\phi L}$	0		$0.3V_{CC}$	V	CLO, Ext. Clk.
Clock Leakage Current High	$I_{L\phi H}$			200	μA	CLO, Ext. Clk. ($V_{OH} = V_{CC}$)
Clock Leakage Current Low	$I_{L\phi L}$			-200	μA	CLO, Ext. Clk. ($V_{OL} = 0V$)
Clock Frequency	f	150		440	KHz	
Clock Rise and Fall Times	tr, tf	0		0.3	μs	Ext. Clk.
Clock Pulse Width	$t_{\phi W}$	0.5		5.6	μs	Ext. Clk.

CAPACITANCE

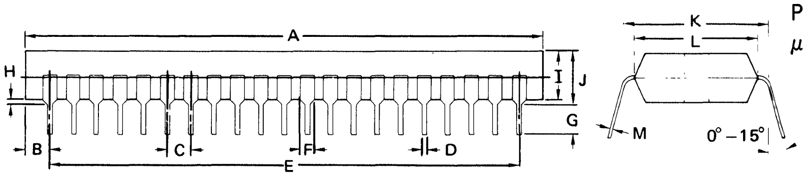
T_a = −30°C to +85°C, V_{CC} = +5V ± 10%.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
I/O Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE μPD651C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

NEC

NEC Microcomputers, Inc.

μPD652

μCOM-45 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD652 is a CMOS version of the μCOM-45. It features a single +5 volt power supply, a 2 mA (max), 800 μA (typ) current drain and extended temperature range. As a μCOM-45, it includes 1000 x 8 ROM, 32 x 4 RAM, and 21 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−30°C to +85°C
Storage Temperature	−55°C to +125°C
Supply Voltage	−0.3 to +7.0 Volts
Input Voltages	−0.3 to +7.0 Volts
Output Voltages	−0.3 to +7.0 Volts
Output Current (Each Output Bit)	2.5 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC/AC CHARACTERISTICS

$T_a = -30°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$.

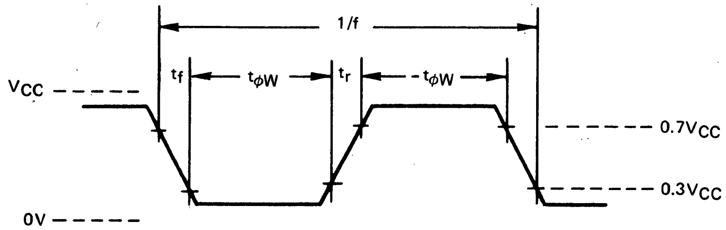
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	$0.7V_{CC}$		V_{CC}	V	Ports A, C, D, $\overline{INT}$, RES
Input Low Voltage	V_{IL}	0		$0.3V_{CC}$	V	Ports A, C, D, $\overline{INT}$, RES
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RES ($V_I = V_{CC}$)
Input Leakage Current Low	I_{LIL}			-10	μA	Ports A, C, D, $\overline{INT}$, RES ($V_I = 0V$)
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D ($V_I = V_{CC}$)
I/O Leakage Current Low	I_{IOL}			-10	μA	Ports C and D ($V_0 = 0_V$)
Output High Voltage 1	V_{OH1}	V_{CC}-0.5			V	Ports C and D (I_{OH} = -1 mA)
		V_{CC}-0.5			V	Ports E to G (I_{OH} = -1 mA)
Output High Voltage 2	V_{OH2}	V_{CC}-2.5			V	Ports C to G (I_{OH} = −2 mA)
Output Low Voltage	V_{OL1}			0.6	V	Ports E to G (I_{OL} = 2 mA)
	V_{OL2}			0.4	V	Ports E to G (I_{OL} = 1.2 mA)
Supply Current	I_{CC}		0.8	2.0	mA	
Clock High Voltage	$V_{\phi H}$	$0.7V_{CC}$		V_{CC}	V	CLO, Ext. Clk.
Clock Low Voltage	$V_{\phi L}$	0		$0.3V_{CC}$	V	CLO, Ext. Clk.
Clock Leakage Current High	$I_{L\phi H}$			200	μA	CLO, Ext. Clk. ($V_{OH} = V_{CC}$)
Clock Leakage Current Low	$I_{L\phi L}$			-200	μA	CLO, Ext. Clk. (V_{OL} = 0V)
Clock Frequency	f	150		440	KHz	
Clock Rise and Fall Times	tr, tf	0		0.3	μs	Ext. Clk.
Clock Pulse Width	$t_{\phi W}$	0.5		5.6	μs	Ext. Clk.

CAPACITANCE

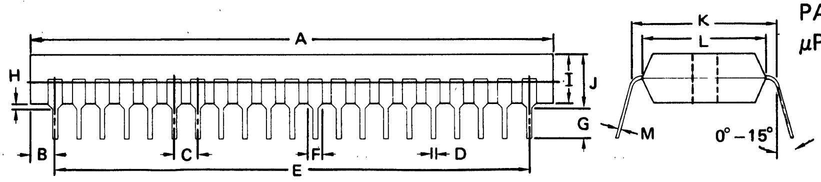
T_a = −30°C to +85°C, V_{CC} = +5V ± 10%.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
I/O Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE
μPD652C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

NEC Microcomputers, Inc.

NEC
μPD556

EVACHIP-43

DESCRIPTION

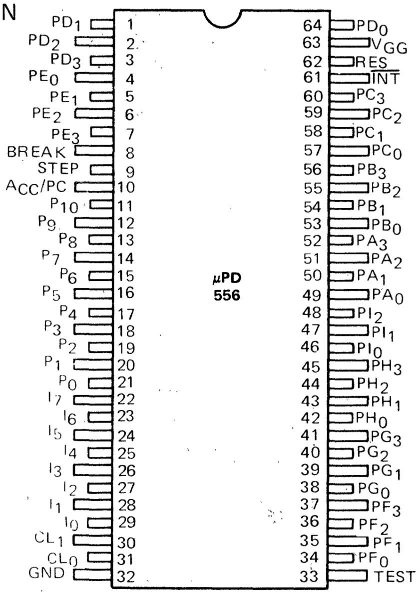
The μPD556 is an evaluation chip for the μCOM-43/44/45 single chip microcomputers. Designed to be used for both hardware and software debugging, the EVACHIP-43 is functionally equivalent to the μCOM-43, except that it does not contain on-chip ROM. Instead, it is able to address external memory. In addition, in order to facilitate debugging, the μPD556 is capable of displaying the contents of the internal accumulator and data pointer and of being single stepped.

When the μPD556 is being used to evaluate μCOM-44/45 designs, the external memory capacity should be restricted to that of the respective on-chip ROM and the instructions should be restricted to the 58 comprising the μCOM-44/45 instruction set.

FEATURES

- 4-bit Parallel Processor
- Full 80 Instruction Set of μCOM-43
- 10 μs Instruction Cycle
- Capable of addressing 2K x 8-bits of external program memory
- Single step capability
- Full Functionality of μCOM-43
- Single supply: −10V PMOS Technology
- Available in a 64-pin Ceramic Quad-in-Line Package

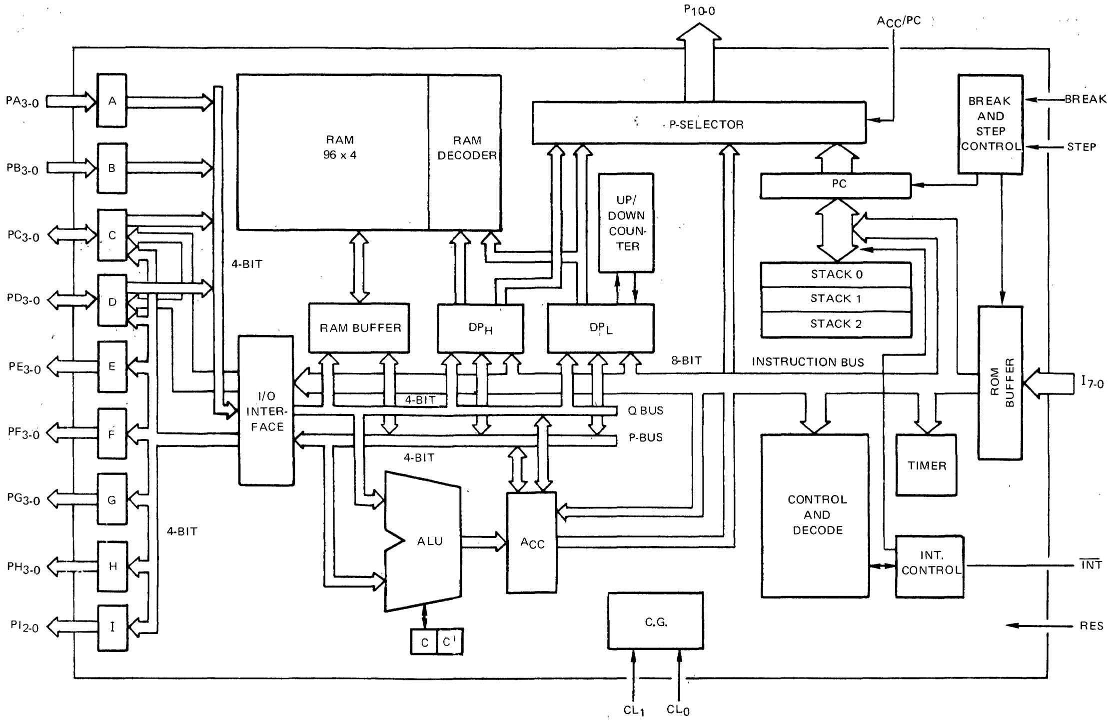
PIN CONFIGURATION



PIN NAMES

PF_0 PF_3	Output Port F
PG_0 PG_3	Output Port G
PH_0 PH_3	Output Port H
PI_0 PI_2	Output Port I
PA_0 - PA_3	Input Port A
PB_0 -- PB_3	Input Port B
PC_0 PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0 - PD_3	Input/Output Port D
PE_0 – PE_3	Output Port E
BREAK	Hold Input
STEP	Single Step Input
A_{CC}/PC	Display A_{CC}/PC Input
P_0 – P_{10}	PC Output
I_0 – I_7	Instruction Input
CL_0 – CL_1	External Clock Source
TEST	Tied to V_{SS} (GND)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage V_{GG}	−15 to +0.3 Volts
All Input Voltages	−15 to +0.3 Volts
All Output Voltages	−15 to +0.3 Volts
Output Current	−4 mA ①

Note: ① All output pins.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

DC CHARACTERISTICS ①

$T_a = -10$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	0		-2.0	V	Port A to D, I_7 to I_0, BREAK, STEP, $\overline{INT}$, RES, and A_{CC}/PC
Input Low Voltage	V_{IL}	-4.3		V_{GG}	V	Port A to D, I_7 to I_0, BREAK, STEP, $\overline{INT}$, RES, and A_{CC}/PC
Clock High Voltage	V_{OH}	0		-0.8	V	CL_0 Input
Clock Low Voltage	V_{OL}	-6.0		V_{GG}	V	CL_0 Input
Input Leakage Current High	I_{LIH}			+10	μA	Port A and B, I_7 to I_0 $\overline{INT}$, RES, BREAK, STEP
				+30	μA	A_{CC}/PC, $V_I = -1V$ Port C and D, $V_I = -1V$
Input Leakage Current Low	I_{LIL}			-10	μA	Port A and B, I_7 to I_0 $\overline{INT}$, RES, BREAK, STEP
				-30	μA	A_{CC}/PC, $V_I = -11V$ Port C and D, $V_I = -11V$
Clock Input Leakage High	I_{LOH}			+200	μA	CL_0 Input, $V_{OH} = 0V$
Clock Input Leakage Low	I_{LOL}			-200	μA	CL_0 Input, $V_{OL} = -11V$
Output High Voltage	V_{OH1}			-1.0	V	Port C to I, P_{10} to P_0 $I_{OH} = -1.0$ mA
	V_{OH2}			-2.3	V	Port C to I, P_{10} to P_0 $I_{OH} = -3.3$ mA
Output Leakage Current Low	I_{LOL}			-30	μA	Port C to I, P_{10} to P_0 $V_0 = -11V$
Supply Current	I_{GG}		-30	-50	mA	

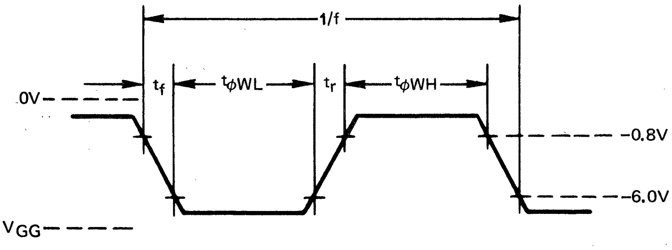
Note: ① Relative to $V_{SS} = 0V$

AC CHARACTERISTICS

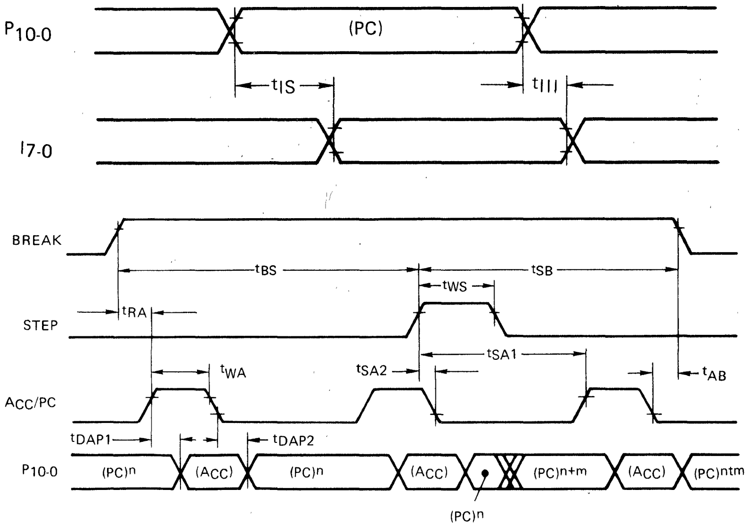
$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Frequency	f	150		440	KHz	
Clock Rise and Fall Times	t_r, t_f	0		0.3	μs	
Clock Pulse Width High	$t_{\phi WH}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi WL}$	0.5		5.6	μs	
Input Setup Time	t_{IS}			5	μs	
Input Hold Time	t_{IH}	0			μs	
BREAK to STEP Interval	t_{BS}	80			tcy	
STEP to RUN Interval	t_{SB}	80			tcy	
STEP Pulse Width	t_{WS}	12			tcy	
BREAK to A_{CC} Interval	t_{BA}	80			tcy	
A_{CC}/PC Pulse Width	t_{WA}	12			tcy	
STEP to A_{CC} Interval	t_{SA1}	80			tcy	
PC to STEP Overlap	t_{SA2}			2	tcy	
PC to RUN Interval	t_{AB}	0			μs	
A_{CC}/PC → P_{10}-P_0 Delay	t_{DAP1}			6	tcy	
	t_{DAP2}			6	tcy	

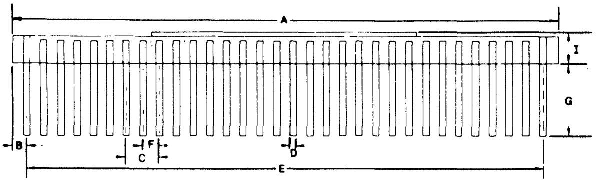
CLOCK WAVEFORM

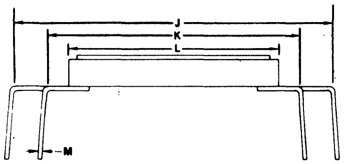


TIMING WAVEFORM



PACKAGE OUTLINE μPD556B





ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002

NEC Microcomputers, Inc.

NEC

μPD551

μCOM-46 SINGLE CHIP MICROCOMPUTER WITH ON-CHIP A/D CONVERTER

DESCRIPTION

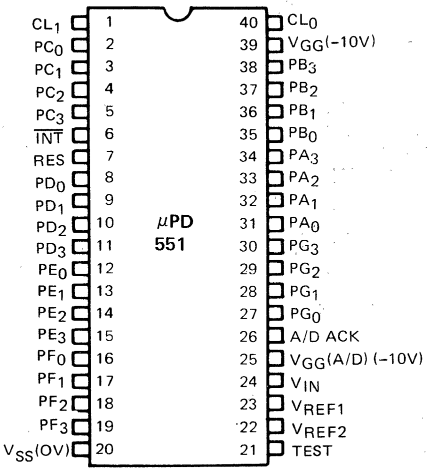
The μCOM-46 is a member of the μCOM-43 Family with an on-chip A/D Converter. Essentially a μCOM-44 with the A/D portion replacing some I/O circuitry, the μCOM-46 has 1000 x 8 ROM, 64 x 4 RAM and 28 I/O lines in addition to the A/D Converter. It is totally software-compatible with the μCOM-44, but does have the additional hardware feature of a two-level stack.

The A/D Converter uses the charge transfer (charge pump) method and the actual conversion is done under software control. The analog input voltage applied to the A/D Converter is obtained as binary digital data with a maximum conversion time of 0.7 msec The level of this applied analog input voltage is then calculated from the binary digital data.

FEATURES

- Stand Alone 4-Bit Microcomputer and A/D Converter
- Powerful 58 Instruction Set
- 10 μs Instruction Cycle
- ROM Size: 1000 x 8
- RAM Size: 64 x 4
- On-Chip A/D Converter: 2% Resolution, 4% Accuracy
- 2 Level Stack
- 28 Input/Output Lines Consisting of: Two 4-Bit Input Ports, Two 4-Bit Input/Outpu Ports and Three 4-Bit Output Ports. All Capable of Both Single-Bit Manipulation and 4-Bit Parallel Processing
- Open Drain Outputs
- P-Channel MOS
- Single Power Supply: −10V
- Available in 40 Pin Plastic Dual-in-Line Package

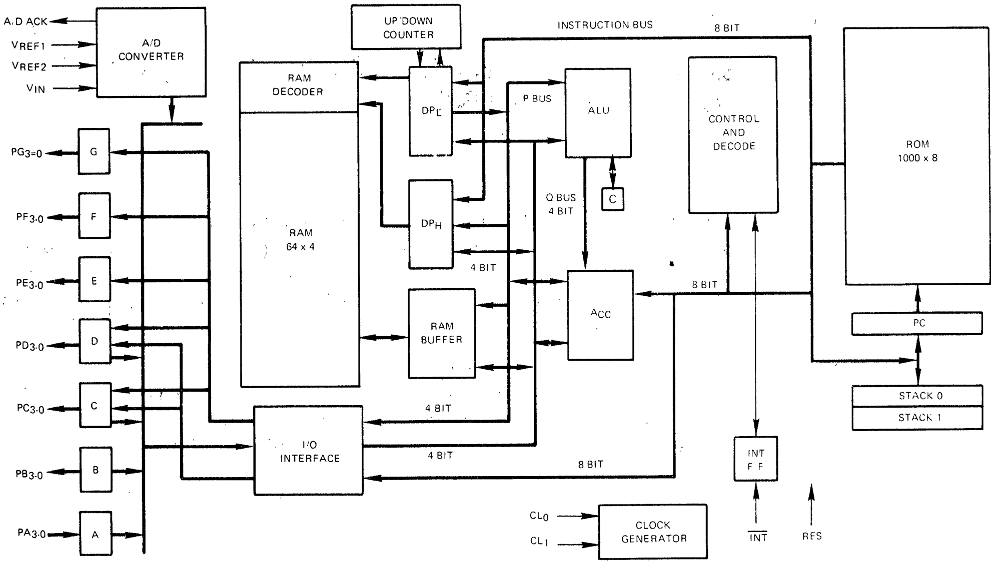
PIN CONFIGURATION



PIN NAMES

CL_0-CL_1	External Clock Source
PC_0-PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
TEST	Input for Testing (Normally GND)
$V_{REF1,2}$	Reference Voltages
V_{IN}	Analog Input Voltage
$V_{GG(A/D)}$	A/D Supply Voltage
A/D ACK	A/D Acknowledge Output
PG_0-PG_3	Output Port G
PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages (Port A, $\overline{\text{INT}}$, RES, TEST)	−15 to +0.3 Volts
(All Other Inputs)	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts
Output Current (Ports C, D)	−4 mA
(Ports E, F, G)	−12 mA
(Total Current)	−60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C.

CAPACITANCE

T_a = 25°C, f = 1 MHz

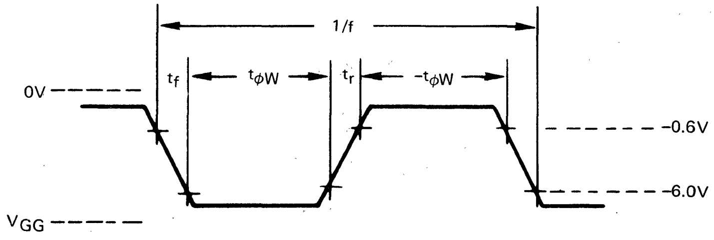
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

DC/AC CHARACTERISTICS

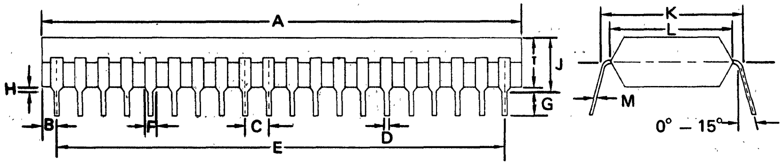
$T_a = -10°C$ to $+70°C$, $V_{GG} = -10V \pm 10\%$.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	0		-2.0	V	Ports A, C, D, $\overline{INT}$, RES
Input Low Voltage	V_{IL1}	-4.5		V_{GG}	V	Ports A, $\overline{INT}$, RES
	V_{IL2}	-4.5		-35	V	Ports C and D
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, $\overline{INT}$, RES, TEST $V_I = 1V$
Input Leakage Current Low	I_{LIL1}			-10	μA	Ports A, $\overline{INT}$, RES, TEST $V_I = -11V$
	I_{LIL2}			-30	μA	Port A $V_I = -35V$
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D $V_I = -1V$
I/O Leakage Current Low	I_{IOL1}			-10	μA	Ports C and D $V_I = -11V$
	I_{IOL2}			-30	μA	Ports C and D $V_I = -35V$
Output Voltage	V_{OH1}			-1.0	V	Ports C and D $I_O = -2$ mA
	V_{OH2}			-2.0	V	Ports E, F, G $I_O = -8$ mA
Output Leakage Current	I_{OL1}			-10	μA	Ports C, D, E, F, G $V_O = -11V$
	I_{OL2}			-30	μA	Ports C, D, E, F, G $V_O = -35V$
Supply Current	I_{GG}		-20	-40	mA	
Clock High Voltage	$V_{\phi H}$	0		-0.6	V	CLO, Ext. Clk.
Clock Low Voltage	$V_{\phi L}$	-6.0		V_{GG}	V	CLO, Ext. Clk.
Clock Leakage Current High	$I_{L\phi H}$			200	μA	CLO, Ext. Clk. ($V_{OH} = V_{CC}$)
Clock Leakage Current Low	$I_{L\phi L}$			-200	μA	CLO, Ext. Clk. ($V_{OL} = 0V$)
Clock Frequency	f	150		440	KHz	
Clock Rise and Fall Times	tr, tf	0		0.3	μs	Ext. Clk.
Clock Pulse Width	$t_{\phi W}$	0.5		5.6	μs	Ext. Clk.

CLOCK WAVEFORM



PACKAGE OUTLINE μPD551C



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.10
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

NEC

NEC Microcomputers, Inc.

µPD780
µPD780-1

8-BIT N-CHANNEL MICROPROCESSOR COMPLETELY Z80™ COMPATIBLE

DESCRIPTION

The µPD780 and µPD780-1 processors are single chip microprocessors developed from third generation technology. Their increased computational power produces higher system through-put and more efficient memory utilization, surpassing that of any second generation microprocessor. The single voltage requirement of the µPD780 and µPD780-1 processors makes it easy to implement them into a system. All output signals are fully decoded and timed to either standard memory or peripheral circuits. An N-channel, ion implanted, silicon gate MOS process is utilized in implementing the circuit.

The block diagram shows the functions of the processor and details the internal register structure. The structure contains 26 bytes of Read/Write (R/W) memory available to the programmer. Included in the registers are two sets of six general purpose registers, which may be used as 8-bit registers individually, or as 16-bit register pairs. Also included are two sets of accumulator and flag registers.

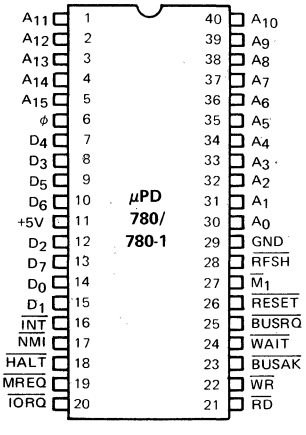
Through a group of exchange instructions the programmer has access to either set of main or alternate registers. The alternate register permits foreground/background mode of operation, or may be used for fast interrupt response. A 16-bit stack pointer is also included in each processor, simplifying implementation of multiple level interrupts, permitting unlimited subroutine nesting, and simplifying many types of data handling.

The two 16-bit index registers simplify implementation of relocatable code and manipulation of tabular data. The Refresh register will automatically refresh external dynamic memories. A powerful interrupt response mode will use the I register to form the upper 8-bits of a pointer to an interrupt service address table, while the interrupting apparatus supplies the lower 8-bits of the pointer. An indirect call will then be made to service this address.

FEATURES

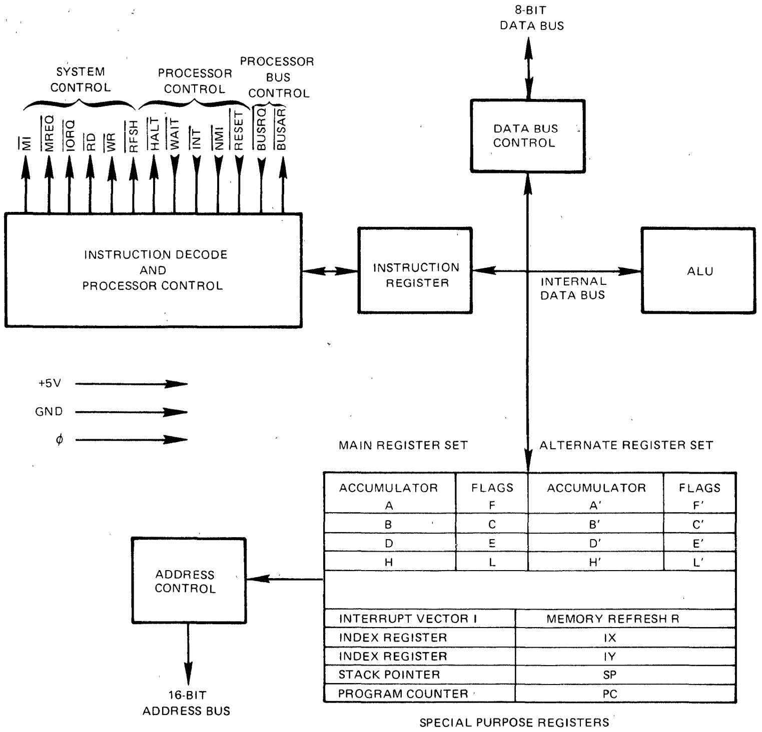
- Single Chip, N-Channel Silicon Gate Processor
- 158 Instructions — Including all 78 of the 8080A Instructions, Permitting Total Software Compatibility
- New 4-, 8-, and 16-Bit Operations Featuring Useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Rapid Interrupt Response, and One Non-Maskable Interrupt
- Directly Connects Standard Speed Dynamic or Static Memories, with Minimum Support Circuitry
- Single-Phase +5 Volt Clock and 5 VDC Supply
- TTL Compatibility
- Automatic Dynamic RAM Refresh Circuitry
- Available in Plastic Package

PIN CONFIGURATION



TM:Z80 is a registered trademark of Zilog, Inc.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN			
NO.	**SYMBOL**	**NAME**	**FUNCTION**
1-5, 30-40	A_0-A_{15}	Address Bus	3-State Output, active high. Pins A_0-A_{15} constitute a 16-bit address bus, which provides the address for memory and I/O device data exchanges. Memory capacity 65,536 bytes. A_0-A_7 is also needed as refresh cycle.
7-10, 12-15	D_0-D_7	Data Bus	3-State input/output, active high. Pins D_0-D_7 compose an 8-bit, bidirectional data bus, used for data exchanges with memory and I/O devices.
27	$\overline{M}_1$	Machine Cycle One	Output, active low. $\overline{M}_1$ indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
19	$\overline{MREQ}$	Memory Request	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
20	$\overline{IORQ}$	Input/Output Request	3-State output, active low. The I/O request signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. The $\overline{IORQ}$ signal is also used to acknowledge an interrupt command, indicating that an interrupt response vector can be placed on the data bus.
21	$\overline{RD}$	Memory Read	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device. The memory or I/O device being addressed should use this signal to gate data onto the data bus.

PIN IDENTIFICATION (CONT.)

PIN			FUNCTION
NO.	SYMBOL	NAME	
22	$\overline{\text{WR}}$	Memory Write	3-State output, active low. The memory write signal indicates that the processor data bus is holding valid data to be stored in the addressed, memory or I/O device.
28	$\overline{\text{RFSH}}$	Refresh	Output, active low. $\overline{\text{RFSH}}$ indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus. The $\overline{\text{MREQ}}$ signal should be used to implement a refresh read to all dynamic memories.
18	$\overline{\text{HALT}}$	Halt State	Output, active low. $\overline{\text{HALT}}$ indicates that the processor has executed a HALT software instruction, and will not resume operation until either a non-maskable or a maskable (with mask enabled) interrupt has been implemented. The processor will execute NOP's while halted, to maintain memory refresh activity.
24	$\overline{\text{WAIT}}$	Wait	Input, active low. $\overline{\text{WAIT}}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. As long as this signal is active, the processor will reenter wait states.
16	$\overline{\text{INT}}$	Interrupt Request	Input, active low. The $\overline{\text{INT}}$ signal is produced by I/O devices. The request will be honored upon completion of the current instruction, if the interrupt enable flip-flop (IFF) is enabled by the internal software. There are three modes of interrupt response. Mode 0 is identical to 8080 interrupt response mode. The Mode 1 response is a restart location at 0038$_H$. Mode 2 is for simple vectoring to an interrupt service routine anywhere in memory.
17	$\overline{\text{NMI}}$	Non-Maskable Interrupt	Input, active low. The non-maskable interrupt has a higher priority than $\overline{\text{INT}}$. It is always acknowledged at the end of the current instruction, regardless of the status of the interrupt enable flip-flop. When the $\overline{\text{NMI}}$ signal is given, the μPD780 processor automatically restarts to location 0066$_H$.
26	$\overline{\text{RESET}}$	Reset	Input, active low. The $\overline{\text{RESET}}$ signal causes the processor to reset the interrupt enable flip-flop (IFF), clear PC and I and R registers, and set interrupt to 8080A mode. During the reset time, the address bus and data bus go to a state of high impedance, and all control output signals become inactive, after which processing continues at 0000H.
25	$\overline{\text{BUSRQ}}$	Bus Request	Input, active low. $\overline{\text{BUSRQ}}$ has a higher priority than $\overline{\text{NMI}}$, and is always honored at the end of the current machine cycle. It is used to allow other devices to take control over the processor address bus, data bus signals; by requesting that they go to a state of high impedance.
23	$\overline{\text{BUSAK}}$	Bus Acknowledge	Output, active low. $\overline{\text{BUSAK}}$ is used to inform the requesting device that the processor address bus, data bus and 3-state control bus signals have entered a state of high impedance, and the external device can now take control of these signals.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin	−0.3 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

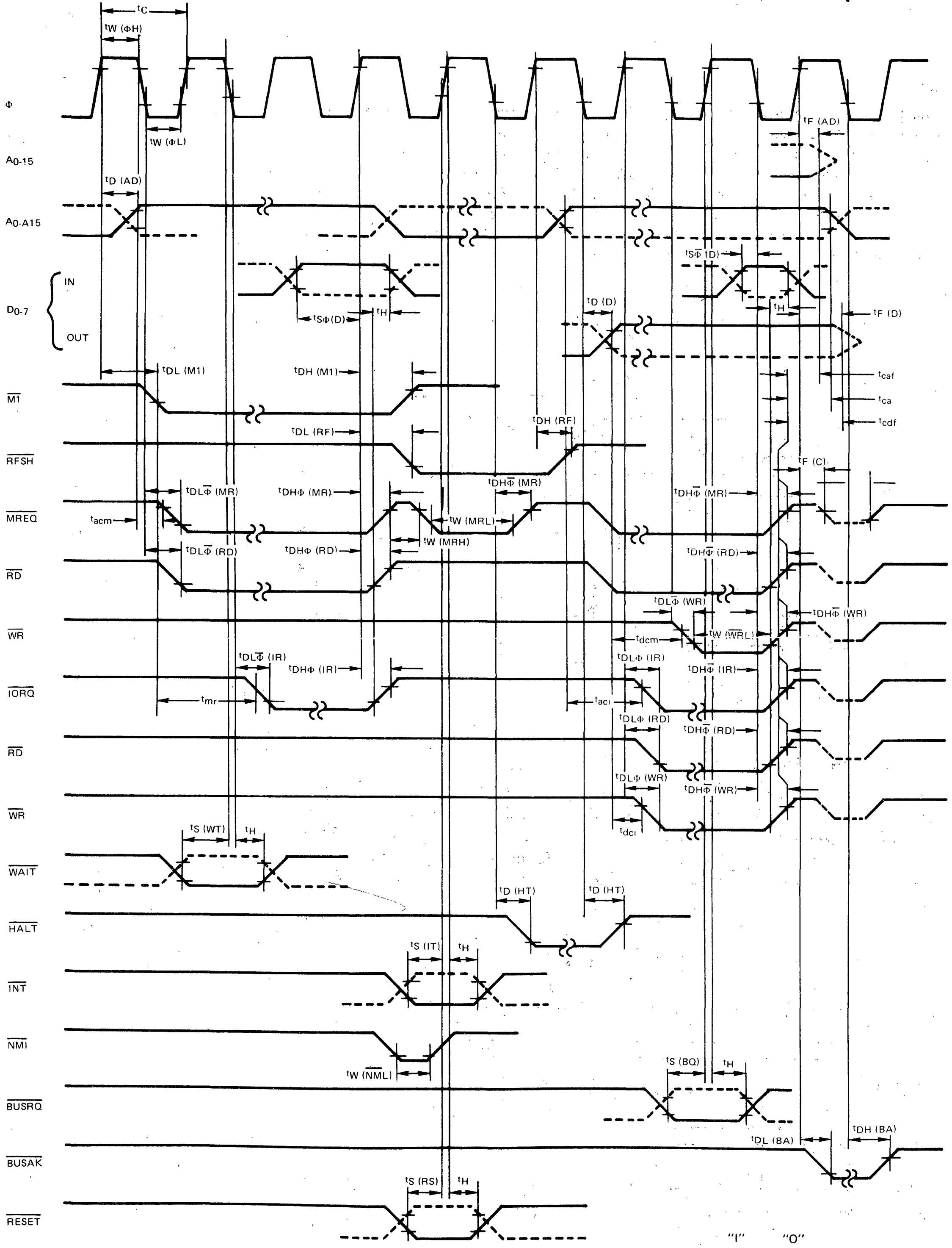
$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

PARAMETER		SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage		V_{ILC}	-0.3		0.45	V	
Clock Input High Voltage		V_{IHC}	V_{cc}-0.2		V_{cc}	V	
Input Low Voltage		V_{IL}	-0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{cc}	V	
Output Low Voltage		V_{OL}			0.4	V	$I_{OL} = 1.8$ mA
Output High Voltage		V_{OH}	2.4			V	$I_{OH} = -250\,\mu A$
Power Supply Current	μPD780	I_{CC}			150	mA	$t_c = 400$ ns
	μPD780-1	I_{CC}		90	200	mA	$t_c = 250$ ns
Input Leakage Current		I_{LI}			10	μA	$V_{IN} = 0$ to V_{cc}
Tri-State Output Leakage Current in Float		I_{LOH}			10	μA	$V_{OUT} = 2.4$ to V_{cc}
Tri-State Output Leakage Current in Float		I_{LOL}			-10	μA	$V_{OUT} = 0.4$ V
Data Bus Leakage Current in Input Mode		I_{LD}			±10	μA	$0 \leqslant V_{IN} \leqslant V_{cc}$

CAPACITANCE

$T_a = 25°C$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ			35	pF	$f_c = 1$ MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured Pins
Output Capacitance	C_{OUT}			10	pF	Returned to Ground

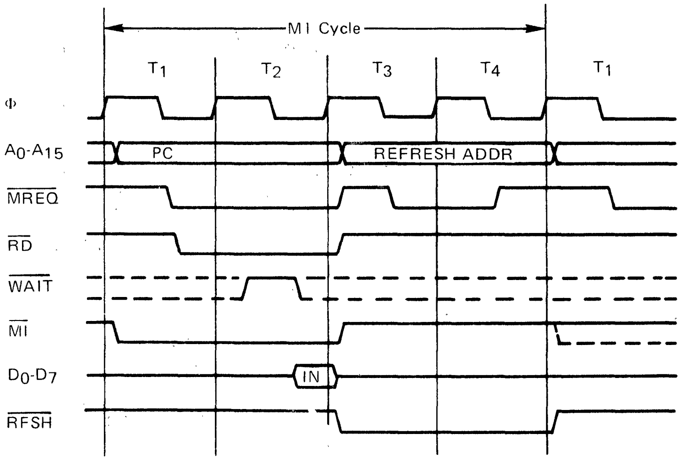


Note: ① Timing measurements are made at the following voltages unless otherwise specified:

	"I"	"O"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	±0.5V

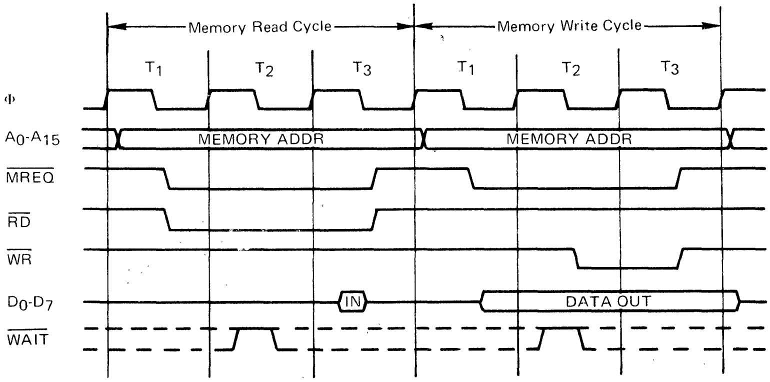
Instruction Op Code Fetch

The contents of the program counter (PC) are placed on the address bus at the start of the cycle. $\overline{MREQ}$ goes active one-half clock cycle later, and the falling edge of this signal can be used directly as a chip enable to dynamic memories. The memory data should be enabled onto the processor data bus when $\overline{RD}$ goes active. The processor takes data with the rising edge of the clock state T_3. The processor internally decodes and executes the instruction, while clock states T_3 and T_4 of the fetch cycle are used to refresh dynamic memories. The refresh control signal $\overline{RFSH}$ indicates that a refresh read should be done to all dynamic memories.



Memory Read or Write Cycles

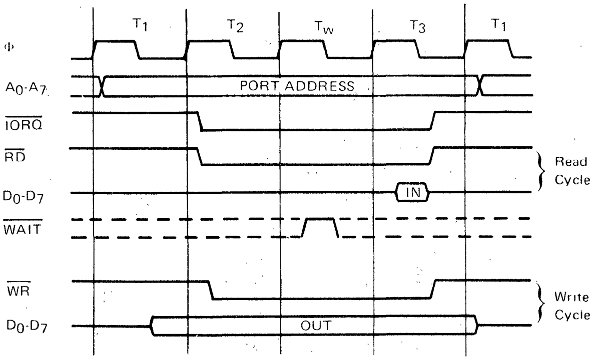
This diagram illustrates the timing of memory read or write cycles other than an op code fetch (M_1 cycle). The function of the $\overline{MREQ}$ and $\overline{RD}$ signals is exactly the same as in the op code fetch cycle. When a memory write cycle is implemented, the $\overline{MREQ}$ becomes active and is used directly as a chip enable for dynamic memories, when the address bus is stable. The $\overline{WR}$ line is used directly as a R W pulse to any type of semiconductor memory, and is active when data on the data bus is stable.



TIMING WAVEFORMS (CONT.)

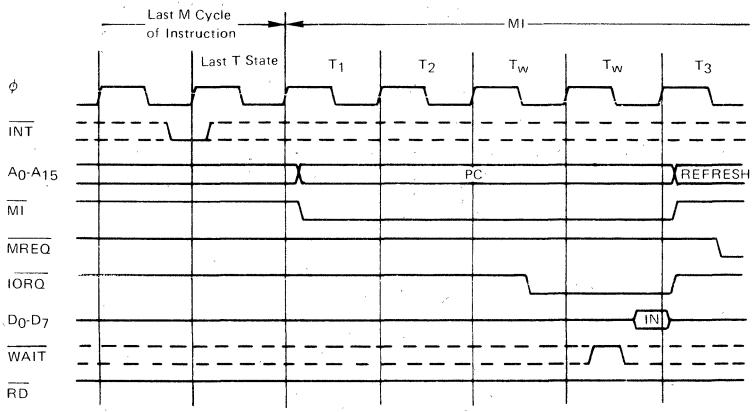
Input or Output Cycles

This illustrates the timing for an I/O read or I/O write operation. A single wait state (T_W) is automatically inserted in I/O operations to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line, if necessary.



Interrupt Request/Acknowledge Cycle

The processor samples the interrupt signal with the rising edge of the last clock at the end of any instruction. A special M_1 cycle is started when an interrupt is accepted. During the M_1 cycle, the $\overline{IORQ}$ (instead of $\overline{MREQ}$) signal becomes active, indicating that the interrupting device can put an 8-bit vector on the data bus. Two wait states (T_W) are automatically added to this cycle. This makes it easy to implement a ripple priority interrupt scheme.



INSTRUCTION SET

The following summary shows the assembly language mnemonic and the symbolic operation performed by the instructions of the µPD780 and µPD780-1 processors. The instructions are divided into 16 categories:

- Miscellaneous Group
- Rotates and Shifts
- Bit Set, Reset and Test
- Input and Output
- Jumps
- Calls
- Restarts
- Returns
- 8-Bit Loads
- 16-Bit Loads
- Exchanges
- Memory Block Moves
- Memory Block Searches
- 8-Bit Arithmetic and Logic
- 16-Bit Arithmetic
- General Purpose Accumulator and Flag Operations

The addressing Modes include combinations of the following:

- Indexed
- Register
- Implied
- Register Indirect
- Bit
- Immediate
- Immediate Extended
- Modified Page Zero
- Relative
- Extended

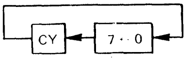
INSTRUCTION SET TABLE

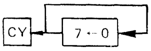
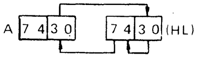
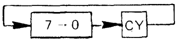
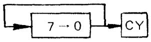
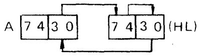
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS						OP CODE
					C	Z	P/V	S	N	H	76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg. pair ss to HL	1	11	↕	↕	V	↕	0	X	11 101 101Ⓐ 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 rrrⒷ
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 nn nnn nnn
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc. (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc. (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 dd ddd ddd
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc. (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 dd ddd ddd
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 nn nnn nnn
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 rrrⒷ
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 dd ddd ddd
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 dd ddd ddd
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss1 001Ⓐ
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101Ⓒ 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101Ⓓ 00 rr1 001
AND r	A ← A∧r	Logical 'AND' of Reg. r ∧ ACC		4	0	↕	P	↕	0	↕	10 100 rrrⒷ
AND n	A ← A∧n	Logical 'AND' of value n ∧ ACC		7	0	↕	P	↕	0	↕	11 100 110 nn nnn nnn
AND (HL)	A ← A∧(HL)	Logical 'AND' of loc. (HL) ∧ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ← A∧(IX + d)	Logical 'AND' of loc. (IX + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 dd ddd ddd
AND (IY + d)	A ← A∧(IY + d)	Logical 'AND' of loc. (IY + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 dd ddd ddd
BIT b, (HL)	Z ← $\overline{(HL)}_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011Ⓔ 01 bbb 110
BIT b, (IX + d)	Z ← $\overline{(IX+d)}_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, (IY + d)	Z ← $\overline{(IY+d)}_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, r	Z ← $\overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011ⒷⒺ 01 bbb rrr
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 100Ⓗ nn nnn nnn nn nnn nnn
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 nn nnn nnn nn nnn nnn
CCF	CY ← CY	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A − r	Compare Reg. r with ACC		4	↕	↕	V	↕	1	↕	10 111 rrrⒷ
CP n	A − n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 nn nnn nnn
CP (HL)	A − (HL)	Compare loc. (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A − (IX + d)	Compare loc. (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 dd ddd ddd
CP (IY + d)		Compare loc. (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 dd ddd ddd
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 101 001
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 111 001

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS						OP CODE
					C	Z	P/V	S	N	H	76 543 210
CPI	A − (HL) HL ← HL + 1 BC ← BC − 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 100 001
CPIR	A − (HL) HL ← HL + 1 BC ← BC − 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 110 001
CPL	A ← A	Complement ACC (1's comp.)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	↕	↕	P	↕	•	↕	00 100 111
DEC r	r ← r − 1	Decrement Reg. r		4	•	↕	V	↕	1	↕	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) − 1	Decrement loc. (HL)		11	•	↕	V	↕	1	↕	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) − 1	Decrement loc. (IX + d)		23	•	↕	V	↕	1	↕	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) − 1	Decrement loc. (IY + d)		23	•	↕	V	↕	1	↕	11 111 101 00 110 101 dd ddd ddd
DEC IX	IX ← IX − 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY − 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss − 1	Decrement Reg. pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B − 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ←e-2→
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF, AF'	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set Interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg. r with input from device (C)	2	12	•	↕	P	↕	0	↕	11 101 101Ⓘ 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	↕	V	↕	0	↕	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	↕	V	↕	0	↕	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	↕	V	↕	0	↕	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg. r	1	4	•	↕	V	↕	0	↕	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B − 1 HL ← HL − 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 010

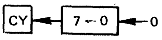
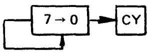
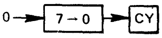
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS						OP CODE
					C	Z	P/V	S	N	H	76 543 210
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	●	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	Load location (HL) with input from port (C); and increment HL and decrement B	2	16	●	↕③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	●	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	●	●	●	●	●	●	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	●	●	●	●	●	●	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	●	●	●	●	●	●	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else continue	Jump to location nn if condition cc is true	3	10	●	●	●	●	●	●	11 ←cc→ 010Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	●	●	●	●	●	●	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met. 12, if not	●	●	●	●	●	●	00 111 000 ←e-2→
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	●	●	●	●	●	●	00 011 000 ←e-2→
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	●	●	●	●	●	●	00 110 000 ←e-2→
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z = 0)	2	7	●	●	●	●	●	●	00 100 000 ←e-2→
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	●	●	●	●	●	●	00 101 000 ←e-2→
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	●	●	●	●	●	●	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	●	●	●	●	●	●	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	●	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	●	●	●	●	●	●	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg. R	2	9	●	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	●	●	●	●	●	●	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	●	●	●	●	●	●	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	●	●	●	●	●	●	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg. pair ss with value nn	4	20	●	●	●	●	●	●	00 ss0 001Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	●	●	●	●	●	●	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg. r	1	7	●	●	●	●	●	●	01 110 rrrⒷ
LD I, A	I ← A	Load I with ACC	2	9	●	●	●	●	●	●	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	●	●	●	●	●	●	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	●	●	●	●	●	●	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	●	●	●	●	●	●	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg. r	3	19	●	●	●	●	●	●	11 011 101Ⓑ 01 110 rrr dd ddd ddd

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS						OP CODE
					C	Z	P/V	S	N	H	76 543 210
LD IY, nn	IY ← nn	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	ss_H ← (nn + 1) ss_L ← (nn)	Load Reg. pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	(IY + d) ← n	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	(IY + d) ← r	Load location (IY + d) with Reg. r	3	19	•	•	•	•	•	•	11 111 101Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	(nn) ← A	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	(nn + 1) ← ss_H (nn) ← ss_L	Load location (nn) with Reg. pair dd	4	20	•	•	•	•	•	•	11 101 101Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	(nn + 1) ← H (nn) ← L	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	R ← A	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	r ← (HL)	Load Reg. r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110Ⓑ
LD r, (IX + d)	r ← (IX + d)	Load Reg. r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	r ← (IY + d)	Load Reg. r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	r ← n	Load Reg. r with value n	2	7	•	•	•	•	•	•	00 rrr 110Ⓑ nn nnn nnn
LD, r, r	r ← r	Load Reg. r with Reg.	1	4	•	•	•	•	•	•	01 rrr r'r'r'Ⓕ
LD SP, HL	SP ← HL	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	SP ← IX	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	SP ← IY	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL)	2	21	•	•	0	•	0	0	11 101 101 10 111 000
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	Load location (DE) with location (HL), increment DE, HL; decrement BC	2	16	•	•	↕①	•	0	0	11 101 101 10 100 000
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL), increment DE, HL; decrement BC and repeat until BC = 0	2	21 if BC ≠ 0 16 if BC = 0	•	•	0	•	0	0	11 101 101 10 110 000
NEG	A ← 0 − A	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS						OP CODE 76 543 210
					C	Z	P/V	S	N	H	
NOP		No operation	1	4	●	●	●	●	●	●	00 000 000
OR r	A ← AV r	Logical 'OR' of Reg. r and ACC		4	0	↕	P	↕	0	↕	10 110 rrr Ⓑ
OR n	A ← AV n	Logical 'OR' of value n and ACC		7	●	↕	P	↕	0	↕	11 110 110 nn nnn nnn
OR (HL)	A ← AV (HL)	Logical 'OR' of loc. (HL) and ACC		7	●	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← (IX + d)	Logical 'OR' of loc. (IX + d) Λ ACC		19	●	↕	P	↕	0	↕	11 011 101 10 110 110 dd ddd ddd
OR (IY + d)	A ← AV (IY + d)	Logical 'OR' of loc. (IY + d) Λ ACC		19	●	↕	P	↕	0	↕	11 111 101 10 110 110 dd ddd ddd
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = 0	●	1	X	X	1	X	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = 0	●	1	X	X	1	X	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg. r	2	12	●	●	●	●	●	●	11 101 101 Ⓑ 01 rrr 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	●	●	●	●	●	●	11 010 011 nn nnn nnn
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	●	↕③	X	X	1	X	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	●	↕③	X	X	1	X	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	●	●	●	●	●	●	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	●	●	●	●	●	●	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg. pair qq with top of stack	1	10	●	●	●	●	●	●	11 qq0 001 Ⓖ
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	●	●	●	●	●	●	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	●	●	●	●	●	●	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg. pair qq onto stack	1	11	●	●	●	●	●	●	11 qq0 101 Ⓖ
RES b, r	S_b ← 0	Reset Bit b of Reg. r		8	●	●	●	●	●	●	11 001 011 Ⓑ 10 bbb rrr Ⓔ
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc. (HL)		15	●	●	●	●	●	●	11 001 011 10 bbb 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc. (IX + d)		23	●	●	●	●	●	●	11 011 101 11 001 011 dd ddd ddd 10 bbb 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc. (IY + d)		23	●	●	●	●	●	●	11 111 101 11 001 011 dd ddd ddd 10 bbb 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	●	●	●	●	●	●	11 001 001
RET cc	If condition cc is false cont. else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	●	●	●	●	●	●	11 ←cc→ 000 Ⓗ
RETI		Return from interrupt	2	14	●	●	●	●	●	●	11 101 101 01 001 101
RETN		Return from non-maskable interrupt	2	14	●	●	●	●	●	●	11 101 101 01 000 101
RL r		Rotate left through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 010 rrr
RL (HL)		Rotate left through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)		Rotate left through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 010 110
RL (IY + d)	m ← r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	●	●	●	0	0	00 010 111

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	↕	↕	P	↕	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg. r left circular	2	8	↕	↕	P	↕	0	0	11 001 011Ⓑ 00 000 rrr
RLCA		Rotate left circular ACC	1	4	↕	●	●	●	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	●	↕	P	↕	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011Ⓑ 00 011 rrr
RR (HL)		Rotate right through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	↕	●	●	●	0	0	00 011 111
RRC r		Rotate Reg. r right circular		2	↕	↕	P	↕	0	0	11 001 011Ⓑ 00 001 rrr
RRC (HL)		Rotate loc. (HL) right circular		4	↕	↕	P	↕	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc. (IX + d) right circular		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate loc. (IY + d) right circular		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	↕	●	●	●	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	●	↕	P	↕	0	0	11 101 101 01 100 111
RST_t	$(SP - 1) \leftarrow PC_H$ $(SP - 2) \leftarrow PC_L$ $PC_H \leftarrow 0, PC_L \leftarrow T$	Restart to location T	1	11	●	●	●	●	●	●	11 ttt 111
SBC A, r	A ← A − r − CY	Subtract Reg. r from ACC w/carry	1	4	↕	↕	V	↕	1	↕	10 011 rrrⒷ
SBC A, n	A ← A − n − CY	Subtract value n from ACC with carry		7	↕	↕	V	↕	1	↕	11 011 110 nn nnn nnn
SBC A, (HL)	A ← A − (HL) − CY	Sub. loc. (HL) from ACC w/carry		7	↕	↕	V	↕	1	↕	10 011 110
SBC A, (IX + d)	A ← A − (IX + d) − CY	Subtract loc. (IX + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A − (IY + d) − CY	Subtract loc. (IY + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL − ss − CY	Subtract Reg. pair ss from HL with carry	2	15	↕	↕	V	↕	1	X	11 101 101Ⓐ 01 ss0 010
SCF	CY ← 1	Set carry flag (C = 1)	1	4	1	●	●	●	0	0	00 110 111
SET b, (HL)	$(HL)_b \leftarrow 1$	Set Bit b of location (HL)	2	15	●	●	●	●	●	●	11 001 011Ⓔ 11 bbb 110
SET b, (IX + d)	$(IX + d)_b \leftarrow 1$	Set Bit b of location (IX + d)	4	23	●	●	●	●	●	●	11 011 101Ⓔ 11 001 011 dd ddd ddd 11 bbb 110

INSTRUCTION SET TABLE (CONT.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	●	●	●	●	●	●	11 111 101Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg. r	2	8	●	●	●	●	●	●	11 001 011Ⓑ 11 bbb rrr
SLA r		Shift Reg. r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011Ⓑ 00 100 rrr
SLA (HL)		Shift loc. (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
SLA (IY + d)		Shift loc. (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg. r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011Ⓑ 00 101 rrr
SRA (HL)		Shift loc. (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
SRA (IY + d)		Shift loc. (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg. r right logical		8	↕	↕	P	↕	0	0	11 001 011Ⓑ 00 111 rrr
SRL (HL)		Shift loc. (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
SRL (IY + d)		Shift loc. (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	$A \leftarrow A - r$	Subtract Reg. r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrrⒷ
SUB n	$A \leftarrow A - n$	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	$A \leftarrow A - (HL)$	Subtract loc. (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	$A \leftarrow A - (IX + d)$	Subtract loc. (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	$A \leftarrow A - (IY + d)$	Subtract loc. (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	$A \leftarrow A \forall r$	Exclusive 'OR' Reg. r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrrⒷ
XOR n	$A \leftarrow A \forall n$	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	$A \leftarrow A \forall (HL)$	Exclusive 'OR' loc. (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	$A \leftarrow A \forall (IX + d)$	Exclusive 'OR' loc. (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	$A \leftarrow A \forall (IY + d)$	Exclusive 'OR' loc. (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES:

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS:

● = Flag not affected
0 = Flag reset
1 = Flag set
X = Flag unknown
↕ = Flag affected according to result of operation
V = Overflow set
P = Parity set
IFF = Interrupt flip-flop set

Ⓐ

Reg	ss
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	rr
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition		Relevant Flag
000	NZ	Non Zero	Z
001	Z	Zero	Z
010	NC	Non Carry	C
011	C	Carry	C
100	PO	Parity Odd	P/V
101	PE	Parity Even	P/V
110	P	Sign Positive	S
111	M	Sign Negative	S

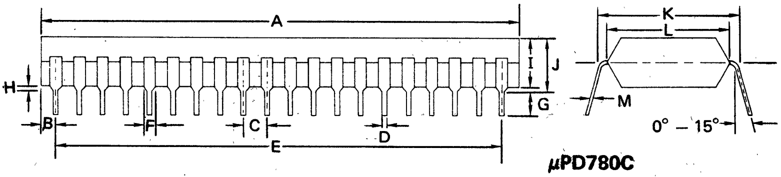
Ⓘ

Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION:

C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

PACKAGE OUTLINES
μPD780C
μPD780C-1



μPD780C
μPD780C-1
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

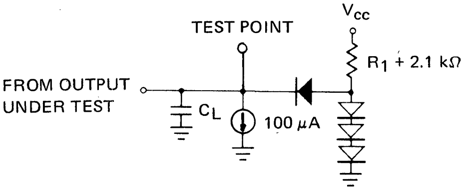
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		μPD780		μPD780-1			
		MIN	MAX	MIN	MAX		
Clock Period	t_c	0.4	⑫	0.25	⑫	μs	
Clock Pulse Width, Clock High	$t_w(\Phi H)$	180		110		ns	
Clock Pulse Width, Clock Low	$t_w(\Phi L)$	180	2000	110	2000	ns	
Clock Rise and Fall Time	$t_{r,f}$		30		30	ns	
Address Output Delay	$t_{D(AD)}$		145		110	ns	$C_L = 50$ pF
Delay to Float	$t_{F(AD)}$		110		90	ns	
Address Stable Prior to $\overline{\text{MREQ}}$ (Memory Cycle)	t_{acm}	①		①		ns	
Address Stable Prior to $\overline{\text{IORQ}}$, $\overline{\text{RD}}$ or $\overline{\text{WR}}$ (I/O Cycle)	t_{aci}	②		②		ns	
Address Stable from $\overline{\text{RD}}$ or $\overline{\text{WR}}$	t_{ca}	③		③		ns	
Address Stable from $\overline{\text{RD}}$ or $\overline{\text{WR}}$ During Float	t_{caf}	④		④		ns	
Data Output Delay	$t_{D(D)}$		230		150	ns	$C_L = 200$ pF
Delay to Float During Write Cycle	$t_{F(D)}$		90		90	ns	
Data Setup Time to Rising Edge of Clock During M1 Cycle	$t_{S\Phi(D)}$	50		35		ns	
Data Setup Time to Falling Edge of Clock During M2 to M5 Cycles	$t_{S\overline{\Phi}(D)}$	60		50		ns	
Data Stable Prior to $\overline{\text{WR}}$ (Memory Cycle)	t_{dcm}	⑤		⑤		ns	
Data Stable Prior to $\overline{\text{WR}}$ (I/O Cycle)	t_{dci}	⑥		⑥		ns	
Data Stable from $\overline{\text{WR}}$	t_{cdf}	⑦		⑦		ns	
Any Hold Time for Setup Time	t_H	0			0	ns	
$\overline{\text{MREQ}}$ Delay from Falling Edge of Clock to $\overline{\text{MREQ}}$ Low	$t_{DL\overline{\Phi}(MR)}$		100		85	ns	$C_L = 50$ pF
$\overline{\text{MREQ}}$ Delay from Rising Edge of Clock to $\overline{\text{MREQ}}$ High	$t_{DH\Phi(MR)}$		100		85	ns	
$\overline{\text{MREQ}}$ Delay from Falling Edge of Clock to $\overline{\text{MREQ}}$ High	$t_{DH\overline{\Phi}(MR)}$		100		85	ns	
Pulse Width, $\overline{\text{MREQ}}$ Low	$t_{w(\overline{MRL})}$	⑧		⑧		ns	
Pulse Width, $\overline{\text{MREQ}}$ High	$t_{w(\overline{MRH})}$	⑨		⑨		ns	
$\overline{\text{IORQ}}$ Delay from Rising Edge of Clock to $\overline{\text{IORQ}}$ Low	$t_{DL\Phi(IR)}$		90		75	ns	
$\overline{\text{IORQ}}$ Delay from Falling Edge of Clock to $\overline{\text{IORQ}}$ Low	$t_{DL\overline{\Phi}(IR)}$		110		85	ns	
$\overline{\text{IORQ}}$ Delay from Rising Edge of Clock to $\overline{\text{IORQ}}$ High	$t_{DH\Phi(IR)}$		100		85	ns	
$\overline{\text{IORQ}}$ Delay from Falling Edge of Clock to $\overline{\text{IORQ}}$ High	$t_{DH\overline{\Phi}(IR)}$		110		85	ns	
$\overline{\text{RD}}$ Delay from Rising Edge of Clock to $\overline{\text{RD}}$ Low	$t_{DL\Phi(RD)}$		100		85	ns	
$\overline{\text{RD}}$ Delay from Falling Edge of Clock to $\overline{\text{RD}}$ Low	$t_{DL\overline{\Phi}(RD)}$		130		95	ns	
$\overline{\text{RD}}$ Delay from Rising Edge of Clock to $\overline{\text{RD}}$ High	$t_{DH\Phi(RD)}$		100		85	ns	
$\overline{\text{RD}}$ Delay from Falling Edge of Clock to $\overline{\text{RD}}$ High	$t_{DH\overline{\Phi}(RD)}$		110		85	ns	
$\overline{\text{WR}}$ Delay from Rising Edge of Clock to $\overline{\text{WR}}$ Low	$t_{DL\Phi(WR)}$		80		65	ns	
$\overline{\text{WR}}$ Delay from Falling Edge of Clock to $\overline{\text{WR}}$ Low	$t_{DL\overline{\Phi}(WR)}$		90		80	ns	
$\overline{\text{WR}}$ Delay from Falling Edge of Clock to $\overline{\text{WR}}$ High	$t_{DH\Phi(WR)}$		100		80	ns	
Pulse Width to $\overline{\text{WR}}$ Low	$t_{w(\overline{WRL})}$	⑩		⑩		ns	
$\overline{\text{MI}}$ Delay from Rising Edge of Clock to $\overline{\text{MI}}$ Low	$t_{DL(MI)}$		130		100	ns	$C_L = 30$ pF
$\overline{\text{MI}}$ Delay from Rising Edge of Clock to $\overline{\text{MI}}$ High	$t_{DH(MI)}$		130		100	ns	
$\overline{\text{RFSH}}$ Delay from Rising Edge of Clock to $\overline{\text{RFSH}}$ Low	$t_{DL(RF)}$		180		130	ns	
$\overline{\text{RFSH}}$ Delay from Rising Edge of Clock to $\overline{\text{RFSH}}$ High	$t_{DH(RF)}$		150		120	ns	
$\overline{\text{WAIT}}$ Setup Time to Falling Edge of Clock	$t_{s(WT)}$	70		70		ns	
$\overline{\text{HALT}}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300	ns	$C_L = 50$ pF
$\overline{\text{INT}}$ Setup Time to Rising Edge of Clock	$t_{s(IT)}$	80		80		ns	
Pulse Width, $\overline{\text{NMI}}$ Low	$t_{w(\overline{NML})}$	80		80		ns	
$\overline{\text{BUSRQ}}$ Setup Time to Rising Edge of Clock	$t_{s(BQ)}$	80		50		ns	
$\overline{\text{BUSAK}}$ Delay from Rising Edge of Clock to $\overline{\text{BUSAK}}$ Low	$t_{DL(BA)}$		120		100	ns	$C_L = 50$ pF
$\overline{\text{BUSAK}}$ Delay from Falling Edge of Clock to $\overline{\text{BUSAK}}$ High	$t_{DH(BA)}$		110		100	ns	
$\overline{\text{RESET}}$ Setup Time to Rising Edge of Clock	$t_{s(RS)}$	90		60		ns	
Delay to Float ($\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$)	$t_{F(C)}$		100		80	ns	
$\overline{\text{MI}}$ Stable Prior to $\overline{\text{IORQ}}$ (Interrupt Ack.)	t_{mr}	⑪		⑪		ns	

Notes:
① $t_{acm} = t_w(\Phi H) + t_f - 65\ (75)^*$
② $t_{aci} = t_c - 70\ (80)^*$
③ $t_{ca} = t_w(\Phi L) + t_r - 50\ (40)^*$
④ $t_{caf} = t_w(\Phi L) + t_r - 45\ (60)^*$
⑤ $t_{dcm} = t_c\ \ 170\ (210)^*$
⑥ $t_{dci} = t_w(\Phi L) + t_r - 170\ (210)^*$
⑦ $t_{cdf} = t_w(\Phi L) + t_r - 70\ (80)^*$
⑧ $t_w(\overline{MRL}) = t_c\ \ 30\ (40)^*$
⑨ $t_w(\overline{MRH}) = t_w(\Phi H) + t_f\ \ 20\ (30)^*$
⑩ $t_w(\overline{WR}) = t_c\ \ 30\ (40)^*$
⑪ $t_{mr} = 2t_c + t_w(\Phi H) + t_f\ \ 65\ (80)^*$
⑫ $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

*These values apply to the μPD780.



LOAD CIRCUIT FOR OUTPUT

NEC Microcomputers, Inc.

NEC

μPD8080AF
μPD8080AF-2
μPD8080AF-1

μPD8080AF 8-BIT N-CHANNEL MIROPROCESSOR FAMILY

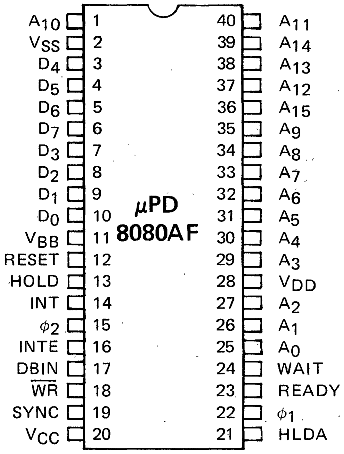
DESCRIPTION

The μPD8080AF is a complete 8-bit parallel processor for use in general purpose digital computer systems. It is fabricated on a single LSI chip using N-channel silicon gate MOS process, which offers much higher performance than conventional microprocessors (1.28 μs minimum instruction cycle). A complete microcomputer system is formed when the μPD8080AF is interfaced with I/O ports (up to 256 input and 256 output ports) and any type or speed of semiconductor memory. It is available in a 40 pin ceramic or plastic package.

FEATURES

- 78 Powerful Instructions
- Three Devices – Three Clock Frequencies
  μPD8080AF – 2.0 MHz
  μPD8080AF-2 – 2.5 MHz
  μPD8080AF-1 – 3.0 MHz
- Direct Access to 64K Bytes of Memory with 16-Bit Program Counter
- 256 8-Bit Input Ports and 256 8-Bit Output Ports
- Double Length Operations Including Addition
- Automatic Stack Memory Operation with 16-Bit Stack Pointer
- TTL Compatible (Except Clocks)
- Multi-byte Interrupt Capability
- **Fully** Compatible with Industry Standard 8080A
- Available in either Plastic or Ceramic Package

PIN CONFIGURATION



Rev/1

FUNCTIONAL DESCRIPTION

The μPD8080AF contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8080AF also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8080AF utilizes a 16-bit address bus to directly address 64K bytes of memory, is fully TTL compatible (1.9 mA), and utilizes the following addressing modes: Direct; Register; Register Indirect; and Immediate.

The μPD8080AF has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8080AF also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

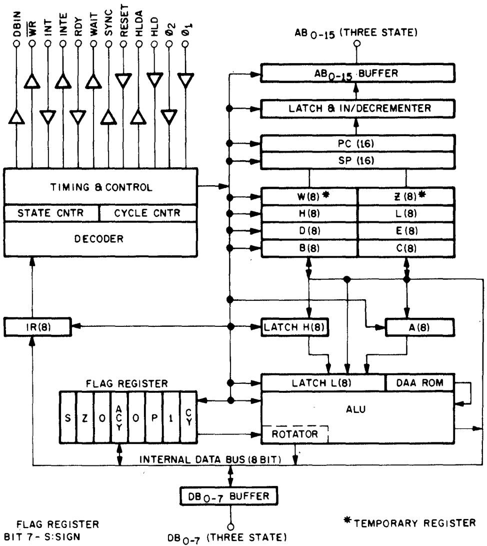
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data busses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All busses, including the control bus, are TTL compatible.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address and data lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8080AF has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This allows the assignment of a separate location for each interrupt operation, and as a result no polling is required to determine which operation is to be performed.

NEC offers three versions of the μPD8080AF. These processors have all the features of the μPD8080AF except the clock frequency ranges from 2.0 MHz to 3.0 MHz. These units meet the performance requirements of a variety of systems while maintaining software and hardware compatibility with other 8080A devices.

BLOCK DIAGRAM



FLAG REGISTER
BIT 7 - S: SIGN
BIT 6 - Z: ZERO
BIT 5 - 0: ALWAYS "0"
BIT 4 - ACY: AUXILIARY CARRY
BIT 3 - 0: ALWAYS "0"
BIT 2 - P: PARITY
BIT 1 - 1: ALWAYS "1"
BIT 0 - CY: CARRY

*TEMPORARY REGISTER

PIN IDENTIFICATION

PIN			
NO.	**SYMBOL**	**NAME**	**FUNCTION**
1, 25-27, 29-40	$A_{15} - A_0$	Address Bus (output three-state)	The address bus is used to address memory (up to 64K 8-bit words) or specify the I/O device number (up to 256 input and 256 output devices). A_0 is the least significant bit.
2	V_{SS}	Ground (input)	Ground
3-10	$D_7 - D_0$	Data Bus (input/ output three-state)	The bidirectional data bus communicates between the processor, memory, and I/O devices for instructions and data transfers. During each sync time, the data bus contains a status word that describes the current machine cycle. D_0 is the least significant bit.
11	V_{BB}	V_{BB} Supply Voltage (input)	−5V ± 5%
12	RESET	Reset (input)	If the RESET signal is activated, the program counter is cleared. After RESET, the program starts at location 0 in memory. The INTE and HLDA flip-flops are also reset. The flags, accumulator, stack pointer, and registers are not cleared. (Note: External synchronization is not required for the RESET input signal which must be active for a minimum of 3 clock periods.)
13	HOLD	Hold (input)	HOLD requests the processor to enter the HOLD state. The HOLD state allows an external device to gain control of the μPD8080AF address and data buses as soon as the μPD8080AF has completed its use of these buses for the current machine cycle. It is recognized under the following conditions: • The processor is in the HALT state. • The processor is in the T_2 or T_W stage and the READY signal is active. As a result of entering the HOLD state, the ADDRESS BUS ($A_{15} - A_0$) and DATA BUS ($D_7 - D_0$) are in their high impedance state. The processor indicates its state on the HOLD ACKNOWLEDGE (HLDA) pin.
14	INT	Interrupt Request (input)	The μPD8080AF recognizes an interrupt request on this line at the end of the current instruction or while halted. If the μPD8080AF is in the HOLD state, or if the Interrupt Enable flip-flop is reset, it will not honor the request.
15	ϕ_2	Phase Two (input)	Phase two of processor clock.
16	INTE ①	Interrupt Enable (output)	INTE indicates the content of the internal interrupt enable flip-flop. This flip-flop is set by the Enable (EI) or reset by the Disable (DI) interrupt instructions and inhibits interrupts from being accepted by the processor when it is reset. INTE is automatically reset (disabling further interrupts) during T_1 of the instruction fetch cycle (M_1) when an interrupt is accepted and is also reset by the RESET signal.
17	DBIN	Data Bus In (output)	DBIN indicates that the data bus is in the input mode. This signal is used to enable the gating of data onto the μPD8080AF data bus from memory or input ports.
18	$\overline{WR}$	Write (output)	$\overline{WR}$ is used for memory WRITE or I/O output control. The data on the data bus is valid while the $\overline{WR}$ signal is active ($\overline{WR} = 0$).
19	SYNC	Synchronizing Signal (output)	The SYNC signal indicates the beginning of each machine cycle.
20	V_{CC}	V_{CC} Supply Voltage (input)	+5V ± 5%
21	HLDA	Hold Acknowledge (output)	HLDA is in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at: • T_3 for READ memory or input operations. • The clock period following T_3 for WRITE memory or OUTPUT operations. In either case, the HLDA appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.
22	ϕ_1	Phase One (input)	Phase one of processor clock.
23	READY	Ready (input)	The READY signal indicates to the μPD8080AF that valid memory or input data is available on the μPD8080AF data bus. READY is used to synchronize the processor with slower memory or I/O devices. If after sending an address out, the μPD8080AF does not receive a high on the READY pin, the μPD8080AF enters a WAIT state for as long as the READY pin is low. (READY can also be used to single step the processor.)
24	WAIT	Wait (output)	The WAIT signal indicates that the processor is in a WAIT state.
28	V_{DD}	V_{DD} Supply Voltage (input)	+12V ± 5%

Note: ① After the EI instruction, the μPD8080AF accepts interrupts on the second instruction following the EI. This allows proper execution of the RET instruction if an interrupt operation is pending after the service routine.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	-65°C to +150°C
Storage Temperature (Plastic Package)	-40°C to +125°C
All Output Voltages ①	-0.3 to +20 Volts
All Input Voltages ①	-0.3 to +20 Volts
Supply Voltages V_{CC}, V_{DD} and V_{SS} ①	-0.3 to +20 Volts
Power Dissipation	1.5W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

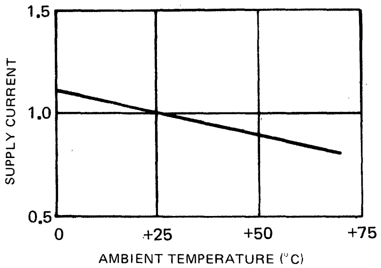
*$T_a = 25°C$

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage	V_{ILC}	V_{SS} - 1		V_{SS} + 0.8	V	
Clock Input High Voltage	V_{IHC}	9.0		V_{DD} + 1	V	
Input Low Voltage	V_{IL}	V_{SS} - 1		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	3.3		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.9 mA on all outputs
Output High Voltage	V_{OH}	3.7			V	I_{OH} = - 150 μA ②
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		40	70	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		60	80	mA	
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			- 100 -2 ②	μA mA	$V_{SS} \leq V_{IN} \leq V_{SS} + 0.8V$ $V_{SS} + 0.8V \leq V_{IN} \leq V_{CC}$
Address and Data Bus Leakage During HOLD	I_{FL}			+10 - 100 ②	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ③



Notes: ① When DBIN is high and $V_{IN} > V_{IH}$ internal active pull-up resistors will be switched onto the data bus.

② Minus (−) designates current flow out of the device.

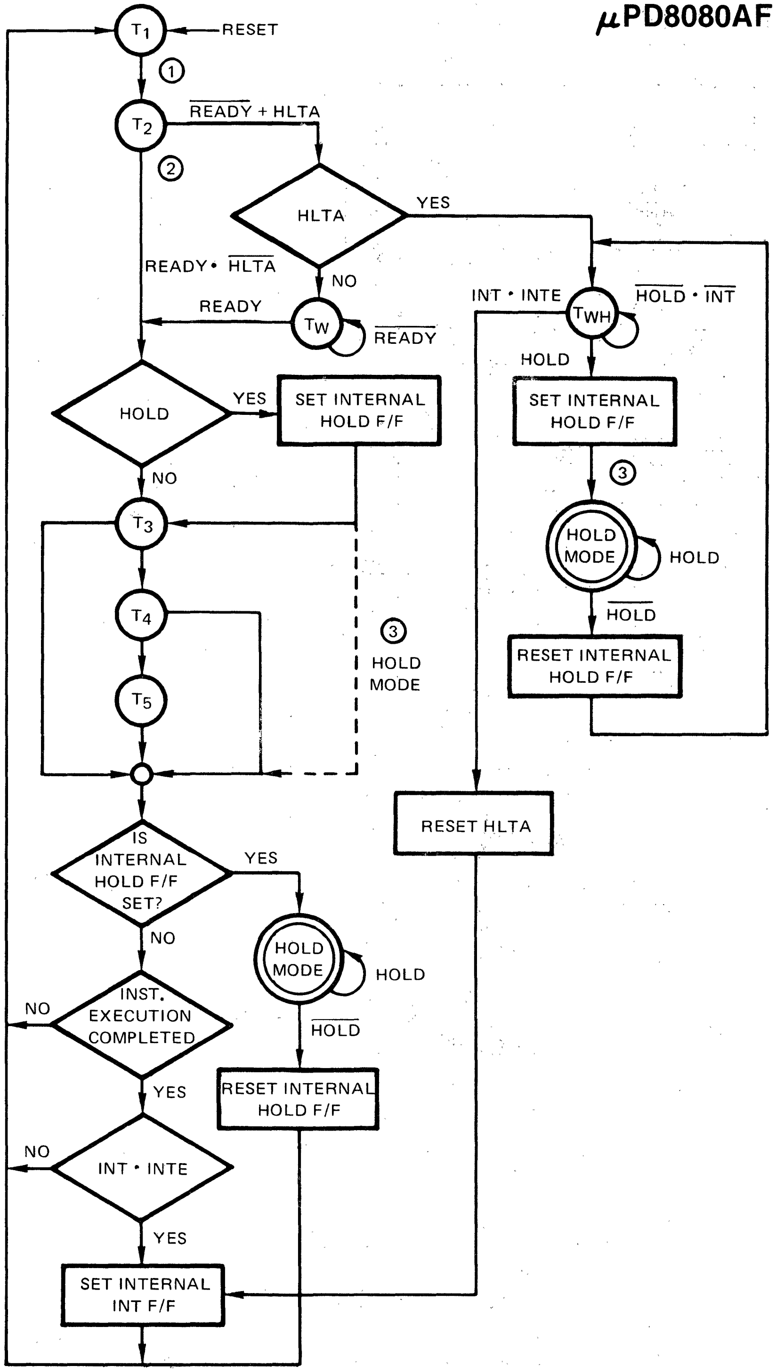
③ ΔI supply/ΔT_a = −0.45%/°C.

CAPACITANCE

T_a = 25°C, $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ		17	25	pF	f_c = 1 MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

PROCESSOR STATE TRANSITION DIAGRAM



Notes:

① INTE F/F IS RESET IF INTERNAL INT F/F IS SET.

② INTERNAL INT F/F IS RESET IF INTE F/F IS RESET.

③ IF REQUIRED, T_4 AND T_5 ARE COMPLETED SIMULTANEOUSLY WITH ENTERING HOLD STATE.

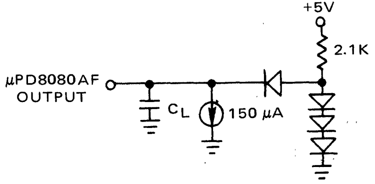
AC CHARACTERISTICS μPD8080AF

$T_a = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.48		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
$\phi 1$ Pulse Width	$t_{\phi 1}$	60			nsec	
$\phi 2$ Pulse Width	$t_{\phi 2}$	220			nsec	
Delay $\phi 1$ to $\phi 2$	t_{D1}	0			nsec	
Delay $\phi 2$ to $\phi 1$	t_{D2}	70			nsec	
Delay $\phi 1$ to $\phi 2$ Leading Edges	t_{D3}	80			nsec	
Address Output Delay From $\phi 2$	t_{DA} ②			200	nsec	$C_L = 100$ pF
Data Output Delay From $\phi 2$	t_{DD} ②			220	nsec	
Signal Output Delay From $\phi 1$, or $\phi 2$ (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	$C_L = 50$ pF
DBIN Delay From $\phi 2$	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During $\phi 1$ and DBIN	t_{DS1}	30			nsec	
Data Setup Time to $\phi 2$ During DBIN	t_{DS2}	150			nsec	
Data Hold Time From $\phi 2$ During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From $\phi 2$	t_{IE} ②			200	nsec	$C_L = 50$ pF
READY Setup Time During $\phi 2$	t_{RS}	120			nsec	
HOLD Setup Time to $\phi 2$	t_{HS}	140			nsec	
INT Setup Time During $\phi 2$ (During $\phi 1$ in Halt Mode)	t_{IS}	120			nsec	
Hold Time from $\phi 2$ (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	$C_L = 100$ pF: Address, Data $C_L = 50$ pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

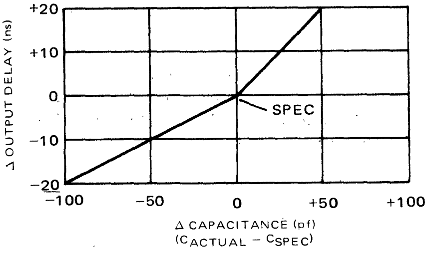
Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. $t_{DH} = 50$ ns or t_{DF}, whichever is less.

② Load Circuit.



③ Actual $t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{f\phi 2} + t_{D2} + t_{r\phi 1} > t_{CY}$ Min.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



AC CHARACTERISTICS
μPD8080AF-2

$T_a = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.38		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi 1}$	60			nsec	
φ2 Pulse Width	$t_{\phi 2}$	175			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	70			nsec	
Address Output Delay From φ2	t_{DA} ②			175	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			200	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	20			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	130			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued:

④ The following are relevant when interfacing the μPD8080AF to devices having $V_{IH} = 3.3V$.

a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.

b. Output delay when measured to 3.0V = SPEC +60 ns at C_L = SPEC.

c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

AC CHARACTERISTICS
μPD8080AF-1

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.32		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		25	nsec	
φ1 Pulse Width	$t_{\phi 1}$	50			nsec	
φ2 Pulse Width	$t_{\phi 2}$	145			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	60			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	60			nsec	
Address Output Delay From φ2	t_{DA} ②			150	nsec	C_L = 50 pF
Data Output Delay From φ2	t_{DD} ②			180	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			110	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		130	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	10			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	120			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 50 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued: ⑤

Device	t_{AW}
μPD8080AF	$2\,t_{CY} - t_{D3} - t_{r\phi 2} - 140$
μPD8080AF-2	$2\,t_{CY} - t_{D3} - t_{r\phi 2} - 130$
μPD8080AF-1	$2\,t_{CY} - t_{D3} - t_{r\phi 2} - 110$

⑥

Device	t_{DW}
μPD8080AF	$t_{CY} - t_{D3} - t_{r\phi 2} - 170$
μPD8080AF-2	$t_{CY} - t_{D3} - t_{r\phi 2} - 170$
μPD8080AF-1	$t_{CY} - t_{D3} - t_{r\phi 2} - 150$

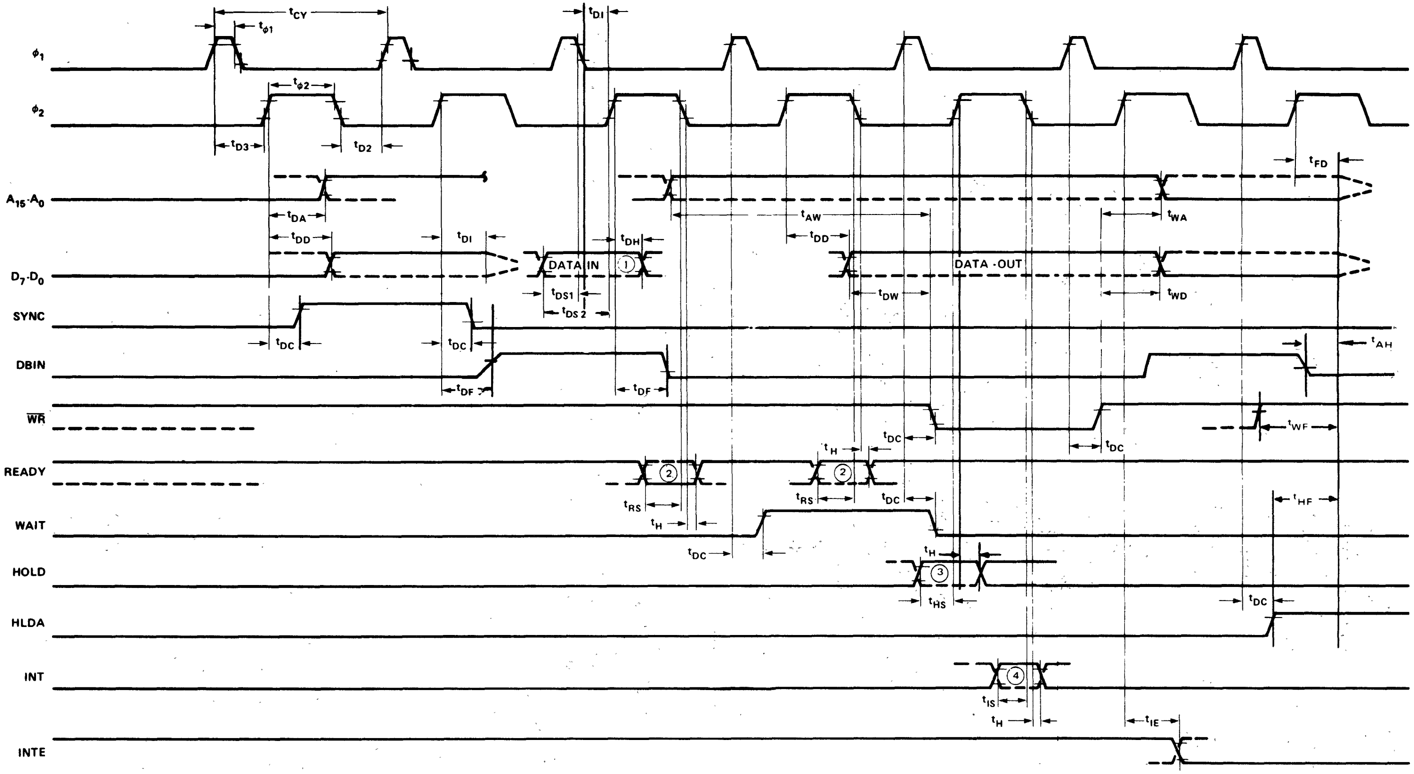
⑦ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi 2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑧ $t_{HF} = t_{D3} + t_{r\phi 2} - 50$ ns.

⑨ $t_{WF} = t_{D3} + t_{r\phi 2} - 10$ ns.

TIMING WAVEFORMS ⑤

(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



Notes: ① Data in must be stable for this period during DBIN • T_3. Both t_{DS1} and t_{DS2} must be satisfied.

② Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)

③ Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)

④ Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized in the following instruction. (External synchronization is not required.)

⑤ This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

⑥ Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8080AF has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8080AF. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8080AF instruction set.

The special instruction group completes the μPD8080AF instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the μPD8080AF is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

One Byte Instructions

									TYPICAL INSTRUCTIONS
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Immediate mode or I/O instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND	

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Jump, call or direct load and store instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2	

INSTRUCTION SET TABLE

		INSTRUCTION CODE[2]									FLAGS[4]			
MNEMONIC[1]	DESCRIPTION	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	5				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	5	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	5	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	17				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	11/17				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	11/17				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	11/17				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	11/17				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	11/17				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	11/17				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	11/17				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	11/17				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	5/11				
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11				
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11				
RC	Return on carry	1	1	0	1	1	0	0	0	5/11				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11				
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11				
RP	Return on positive	1	1	1	1	0	0	0	0	5/11				
RM	Return on minus	1	1	1	1	1	0	0	0	5/11				

		INSTRUCTION CODE[2]									FLAGS[4]			
MNEMONIC[1]	DESCRIPTION	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	11				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	11				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	11				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	11				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	5				
INX D	Increment DE	0	0	0	1	0	0	1	1	5				
INX H	Increment HL	0	0	1	0	0	0	1	1	5				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	5				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	5				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	5				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	5				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	5				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	18				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	5				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	5				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RST A	Restart	1	1	A	A	A	1	1	1	11				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				$\overline{Cy}$
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	7				

Notes.

[1] Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101L – 110 Memory – 111 A.

[3] Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
= flag not affected
0 = flag reset
1 = flag set

INSTRUCTION CYCLE TIMES

One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During $\phi_1 \cdot$ SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 ① SPW3 ⑤ SPW3 ⑤	11
All CALL Instructions	PCR5 ① PCR3 ② PCR3 ② SPW3 ⑤ SPW3 ⑤	11/17
Conditional TURN Instructions	PCR5 ① SPR3 ④ SPR3 ④	5/11
RET Instruction	PCR4 ① SPR3 ④ SPR3 ④	10
XTHL	PCR4 ① SPR3 ④ SPR3 ④ SPW3 ⑤ SPW5 ⑤	18
DAD RP	PCR4 ① PCX3 ⓧ PCX3 ⓧ	10
INR R; INX RP, DCR R; DCX RP; PCHL; MOV R, R; SPHL	PCR5 ①	5
All JUMP Instructions and LXI RP	PCR4 ① PCR3 ② PCR3 ②	10
POP RP LDA STA LHLD SHLD	PCR4 ① SPR3 ④ SPR3 ④ PCR4 ① PCR3 ② PCR3 ② BBR3 ② PCR4 ① PCR3 ② PCR3 ② BBW3 ③ PCR4 ① PCR3 ② PCR3 ② BBR3 ② BBR3 ② PCR4 ① PCR3 ② PCR3 ② BBW3 ③ BBW3 ③	10 13 13 16 16
STAX B STAX D LDAX B LDAX D	PCR4 ① BCW3 ③ PCR4 ① DEW3 ③ PCR4 ① BCR3 ② PCR4 ① DER3 ②	7 7 7 7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 ① HLR3 ②	7
INR M and DCR M	PCR4 ① HLR3 ② HLW3 ③	10
MVI M	PCR4 ① PCR3 ② HLW3 ③	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 ① PCR3 ②	7
MOV M, R	PCR4 ① HLW3 ③	7
EI; DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG	PCR4 ①	4
OUT IN HLT	PCR4 ① PCR3 ② ABW3 ⑦ PCR4 ① PCR3 ② ABR3 ⑥ PCR4 ① PCX3 ⑨	10 10 7

Machine Cycle Symbol Definition

XX Y Z Ⓝ
Ⓝ → Status word defining type of machine cycle (See Status Word Chart)
Z → Number of clocks for this machine cycle
Y → R = Read cycle – data into processor
W = Write cycle – data out of processor
X = No data transfer
XX → PC = Program Counter used as address

XX → HL = Registers H and L used as address
BC = Registers B and C used as address
DE = Registers D and E used as address
SP = Stack Pointer used as address
BB = Byte 2 and 3 used as address
AB = Byte 2 used as address

Underlined (XXYZⓃ) indicates machine cycle is executed if condition is True.

STATUS INFORMATION DEFINITION

SYMBOLS	DATA BUS BIT	DEFINITION
INTA ①	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart or CALL instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP ①	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR ①	D_7	Designates that the data bus will be used for memory read data.

Note: ① These three status bits can be used to control the flow of data onto the μPD8080AF data bus.

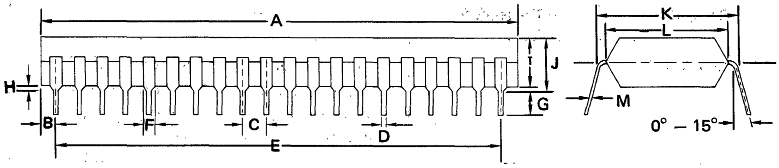
STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE	HALT ACKNOWLEDGE	INT. ACK. WHILE HALT
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

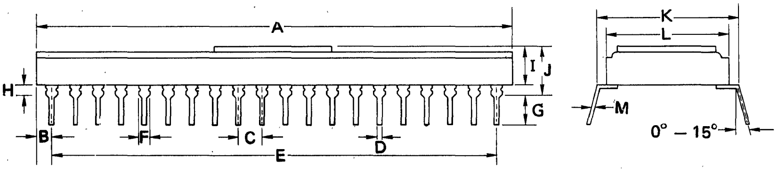
Ⓝ STATUS WORD

PACKAGE OUTLINE
μPD8080AFC/D



μPD8080AFC
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.10
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8080AFD
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.100
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.5	0.531
M	0.30 ± 0.1	0.012 ± 0.004

NEC Microcomputers, Inc.

NEC
μPD8085A

μPD8085A SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

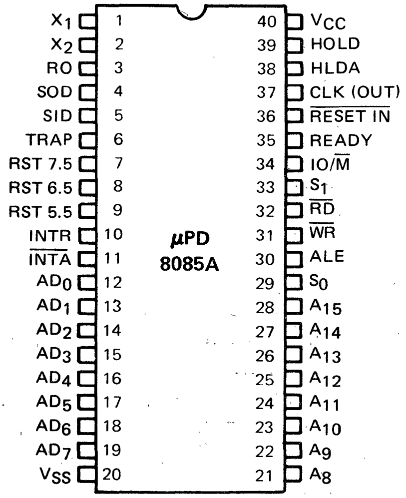
DESCRIPTION

The μPD8085A is a single chip 8-bit microprocessor which is 100 percent software compatible with the industry standard 8080A. It has the ability of increasing system performance of the standard 8080A by operating at a higher speed. Using the μPD8085A in conjunction with its family of ICs allows the designer complete flexibility with minimum chip count.

FEATURES

- Single Power Supply: +5 Volt
- Internal Clock Generation and System Control
- Internal Serial In/Out Port.
- Fully TTL Compatible
- Internal 4-Level Interrupt Structure
- Multiplexed Address/Data Bus for Increased System Performance
- Complete Family of Components for Design Flexibility
- Software Compatible with Standard 8080A
- Available in Either Plastic or Ceramic Package

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The μPD8085A contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8085A also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8085A has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8085A also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

The μPD8085A was designed with speed and simplicity of the overall system in mind. The multiplexed address/data bus increases available pins for advanced functions in the processor and peripheral chips while providing increased system speed and less critical timing functions. All signals to and from the μPD8085A are fully TTL compatible.

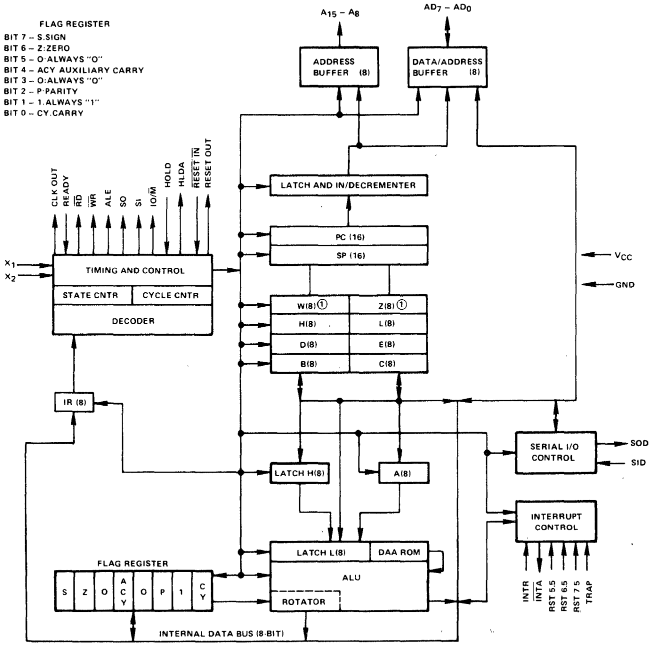
The internal interrupt structure of the μPD8085A features 4 levels of prioritized interrupt with three levels internally maskable.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address, data and control lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8085A features internal clock generation with status outputs available for advanced read/write timing and memory/IO instruction indications. The clock may be crystal controlled, RC controlled, or driven by an external signal.

On chip serial in/out port is available and controlled by the newly added RIM and SIM instructions.

BLOCK DIAGRAM



Note ①TEMPORARY REGISTER

PIN IDENTIFICATION

PIN			
NO.	**SYMBOL**	**NAME**	**FUNCTION**
1, 2	X_1, X_2	Crystal In	Crystal, RC, or external clock input
3	RO	Reset Out	Acknowledge that the processor is being reset to be used as a system reset
4	SOD	Serial Out Data	1-bit data out by the SIM instruction
5	SID	Serial In Data	1-bit data into ACC bit 7 by the RIM instruction
6	Trap	Trap Interrupt Input	Highest priority nonmaskable restart interrupt
7 8 9	RST 7.5 RST 6.5 RST 5.5	Restart Interrupts	Priority restart interrupt inputs, of which 7.5 is the highest and 5.5 the lowest priority
10	INTR	Interrupt Request In	A general interrupt input which stops the PC from incrementing, generates $\overline{\text{INTA}}$, and samples the data bus for a restart or call instruction
11	$\overline{\text{INTA}}$	Interrupt Acknowledge	An output which indicates that the processor has responded to INTR
12-19	$AD_0 - AD_7$	Low Address/Data Bus	Multiplexed low address and data bus
20	V_{SS}	Ground	Ground Reference
21-28	$A_8 - A_{15}$	High Address Bus	Nonmultiplexed high 8-bits of the address bus
29, 33	S_0, S_1	Status Outputs	Outputs which indicate data bus status: Halt, Write, Read, Fetch
30	ALE	Address Latch Enable Out	A signal which indicates that the lower 8-bits of address are valid on the AD lines
31, 32	$\overline{\text{WR}}$, $\overline{\text{RD}}$	Write/Read Strobes Out	Signals out which are used as write and read strobes for memory and I/O devices
34	IO/$\overline{\text{M}}$	I/O or Memory Indicator	A signal out which indicates whether $\overline{\text{RD}}$ or $\overline{\text{WR}}$ strobes are for I/O or memory devices
35	Ready	Ready Input	An input which is used to increase the data and address bus access times (can be used for slow memory)
36	$\overline{\text{Reset In}}$	Reset Input	An input which is used to start the processor activity at address 0, resetting IE and HLDA flip-flops
37	CLK	Clock Out	System Clock Output
38, 39	HLDA, HOLD	Hold Acknowledge Out and Hold Input Request	Used to request and indicate that the processor should relinquish the bus for DMA activity. When hold is acknowledged, $\overline{\text{RD}}$, $\overline{\text{WR}}$, IO/$\overline{\text{M}}$, Address and Data busses are all 3-stated.
40	V_{CC}	5V Supply	Power Supply Input

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
(Plastic Package)	−40°C to +125°C
All Output Voltages	−0.3 to +7 Volts
All Input Voltages	−0.3 to +7 Volts
Supply Voltage V_{CC}	−0.3 to +7 Volts
Power Dissipation	1.5W

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, V_{SS} = GND, unless otherwise specified

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V_{IL}	$V_{SS} - 0.5$		$V_{SS} + 0.8$	V	
Input High Voltage	V_{IH}	2.0		$V_{CC} + 0.5$	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA on all outputs
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400\ \mu s$ ①
Power Supply Current (V_{CC})	I_{CC} (AV)			170	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ①	μA	$V_{IN} = V_{CC}$
Output Leakage	I_{LO}			±10 ①	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
Input Low Level, Reset	V_{ILR}	−0.5		+0.8	V	
Input High Level, Reset	V_{IHR}	2.4		$V_{CC} + 0.5$	V	
Hysteresis, Reset	V_{HY}	0.25			V	

Note: ① Minus (−) designates current flow out of the device.

AC CHARACTERISTICS

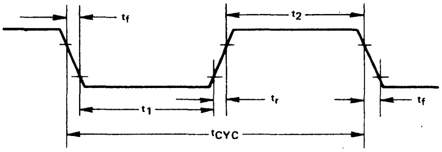
$T_a = 0^\circ C$ to $+70^\circ C$; $V_{CC} = 5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
CLK Cycle Period	T_{CYC}	320		2000	ns	
CLK Low Time	t_1	80			ns	
CLK High Time	t_2	120			ns	
CLK Rise and Fall Time	t_r, t_f			30	ns	$T_{CYC} = 320$ ns
Address Valid Before Trailing Edge of ALE	t_{AL}	110			ns	$C_L = 150$ pF
Address Hold Time After ALE	t_{LA}	100			ns	
ALE Width	t_{LL}	140			ns	
ALE Low During CLK High	t_{LCK}	100			ns	Output Voltages:
Trailing Edge of ALE to Leading Edge of Control	t_{LC}	130			ns	$V_L = 0.8$ Volts $V_H = 2.0$ Volts
Address Float After Leading Edge of $\overline{\text{READ}}$ ($\overline{\text{INTA}}$)	t_{AFR}			0	ns	
Valid Address to Valid Data In	t_{AD}			575	ns	Input Voltages:
$\overline{\text{READ}}$ (or $\overline{\text{INTA}}$) to Valid Data	t_{RD}			300	ns	$V_L = 0.8$ Volts
Data Hold Time After $\overline{\text{READ}}$ ($\overline{\text{INTA}}$)	t_{RDH}	0			ns	$V_H = 1.5$ Volts at 20 ns rise and fall times
Trailing Edge of $\overline{\text{READ}}$ to Re-Enabling of Address	t_{RAE}	150			ns	
Address (A_8-A_{15}) Valid After Control ①	t_{CA}	120			ns	For outputs where $C_L \neq 150$ pf, correct as follows:
Data Valid to Trailing Edge of $\overline{\text{WRITE}}$	t_{DW}	420			ns	
Data Valid After Trailing Edge of $\overline{\text{WRITE}}$	t_{WD}	100			ns	$25 \text{ pf} \leq C_L \leq 150 \text{ pf}$ 0.10 ns/pf
Width of Control Low ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{INTA}}$)	t_{CC}	400			ns	
Trailing Edge of Control to Leading Edge of ALE	t_{CL}	50			ns	
READY Valid from Address Valid	t_{ARY}			220	ns	$150 \text{ pf} \leq C_L \leq 300 \text{ pf}$ + 0.30 ns/pf
READY Setup Time to Leading Edge of CLK	t_{RYS}	110			ns	
READY Hold Time	t_{RYH}	0			ns	
HLDA Valid to Trailing Edge of CLK	t_{HACK}	110			ns	Outputs measured with only capacitive load
Bus Float After HLDA	t_{HABF}			210	ns	
HLDA to Bus Enable	t_{HABE}			210	ns	
ALE to Valid Data In	t_{LDR}			460	ns	
Control Trailing Edge to Leading Edge of Next Control	t_{RV}	400			ns	
Address Valid to Leading Edge of Control	t_{AC}	270			ns	
HOLD Setup Time to Trailing Edge of CLK	t_{HDS}	170			ns	
HOLD Hold Time	t_{HDH}	0			ns	
INTR Setup Time to Leading Edge of CLK (M1, T1 only). Also RST and TRAP	t_{INS}	160			ns	
INTR Hold Time	t_{INH}	0			ns	

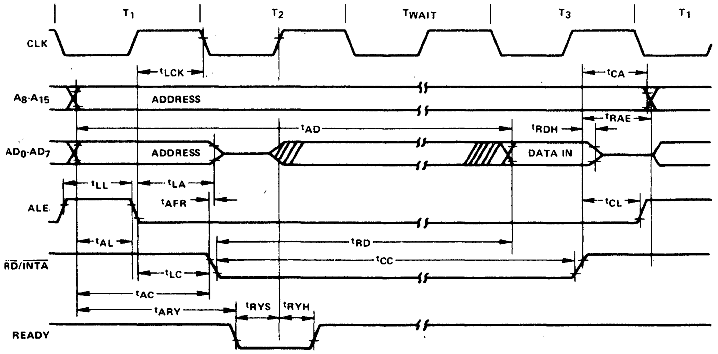
Note: ① IO/$\overline{\text{M}}$, SO, SI

TIMING WAVEFORMS

CLOCK TIMING

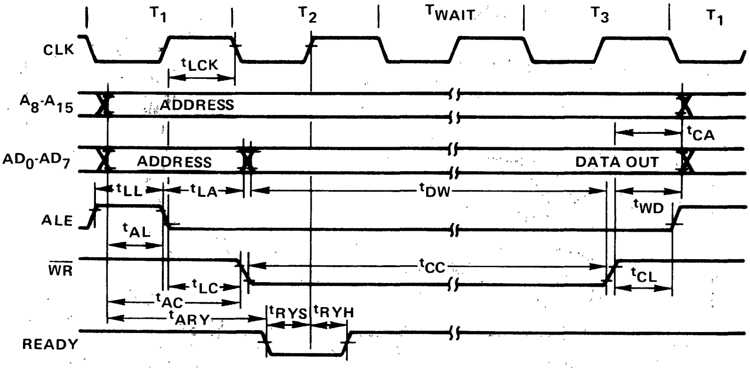


READ OPERATION

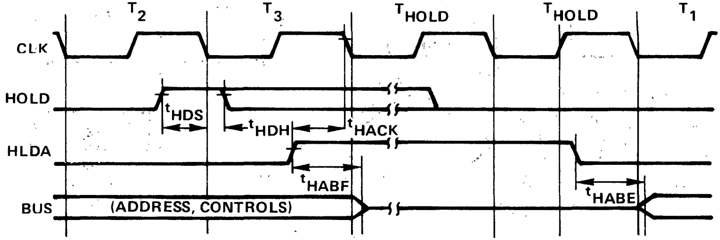


TIMING WAVEFORMS (CONT.)

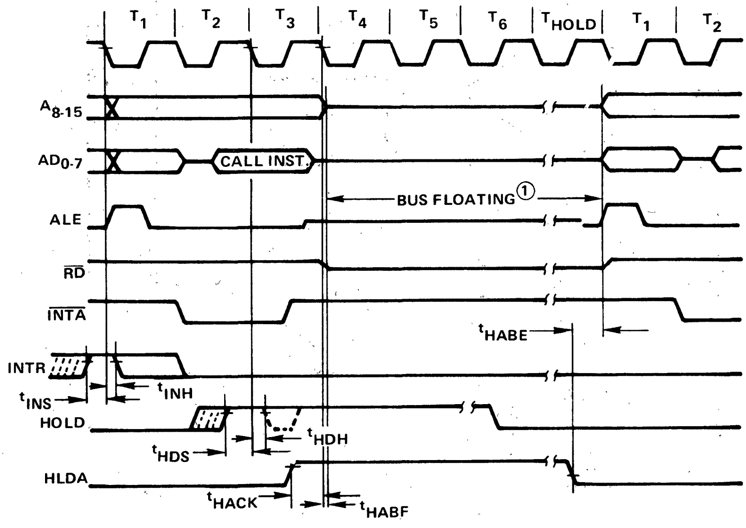
WRITE OPERATION



HOLD OPERATION

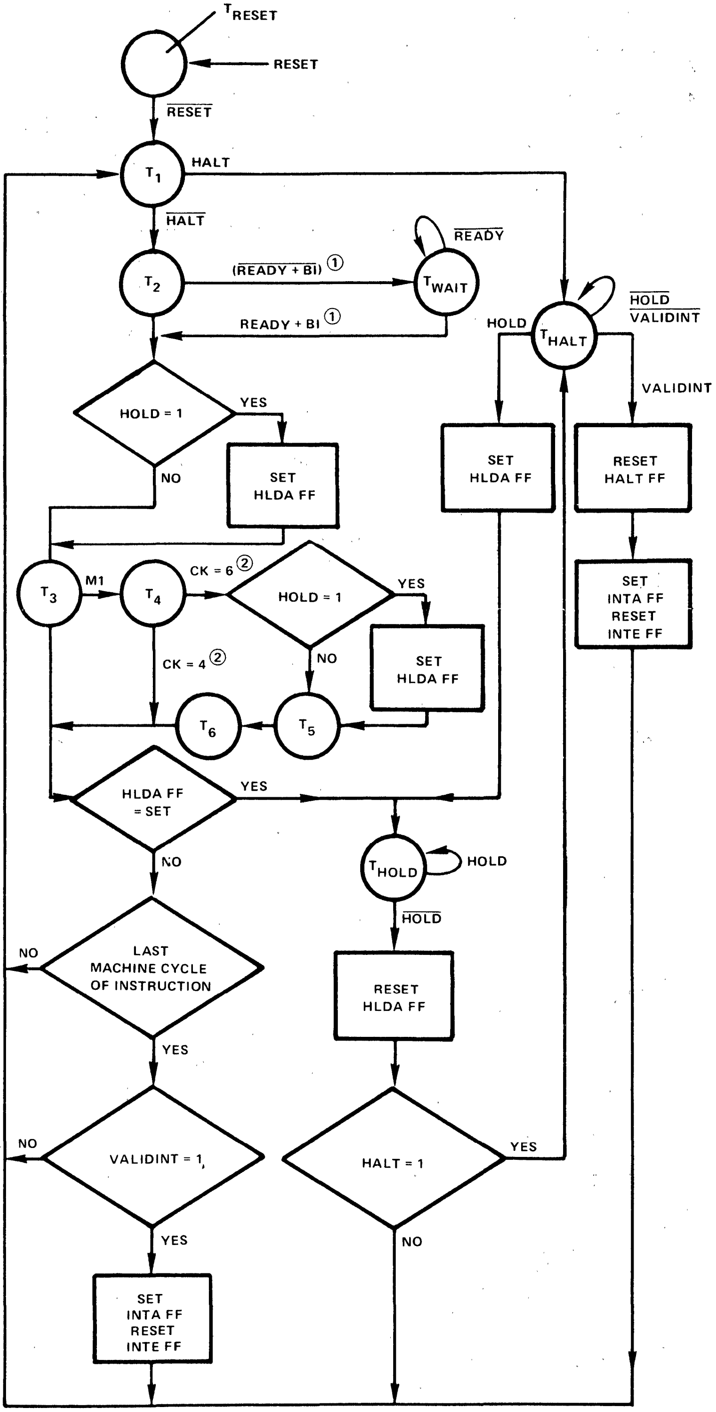


INTERRUPT TIMING



Note:① IO/M̄ is also floating during this time.

PROCESSOR STATE TRANSITION DIAGRAM



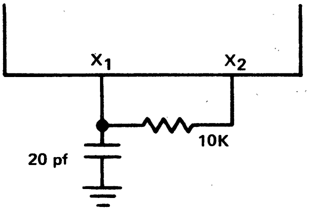
Notes: ① BI indicates that the bus is idle during this machine cycle.

② CK indicates the number of clock cycles in this machine cycle.

CLOCK INPUTS ①

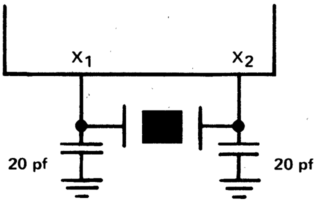
As stated, the timing for the μPD8085A may be generated in one of three ways; crystal, RC, or external clock. Recommendations for these methods are shown below.

RC



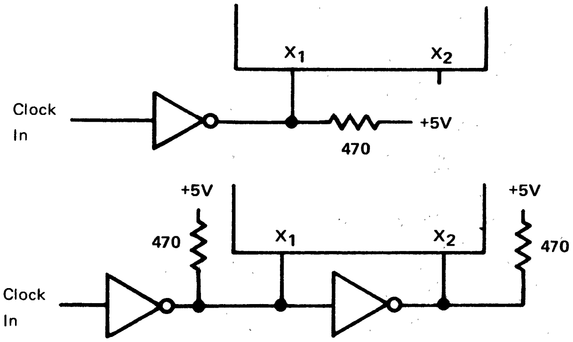
≈3 MHz Input Frequency
RC Resonance

CRYSTAL



1-6 MHz Input Frequency
Parallel Resonant Crystal

EXTERNAL



1-6 MHz 25-50% DC
X_2 not used

1-6 MHz > 50% DC

Note: ① Input frequency must be twice the internal operating frequency.

STATUS OUTPUTS

The Status Outputs are valid during ALE time and have the following meaning:

	S1	S0
Halt	0	0
Write	0	1
Read	1	0
Fetch	1	1

These pins may be decoded to portray the processor's data bus status.

INTERRUPTS

The μPD8085A has five interrupt pins available to the user. INTR is operationally the same as the 8080 interrupt request, three (3) internally maskable restart interrupts: RESTART 5.5, 6.5 and 7.5, and TRAP, a nonmaskable restart.

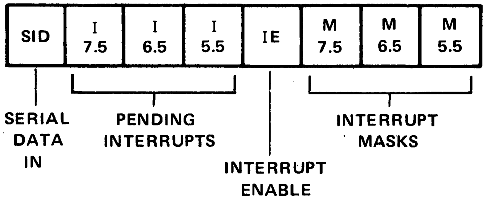
PRIORITY	INTERRUPT	RESTART ADDRESS
Highest	TRAP	24_{16}
|	RST 5.5	$2C_{16}$
|	RST 6.5	34_{16}
|	RST 7.5	$3C_{16}$
Lowest	INTR	

INTR, RST 5.5 and RST 6.5 are all level sensing inputs while RST 7.5 is set on a rising edge. TRAP, the highest priority interrupt, is nonmaskable and is set on the rising edge or positive level. It must make a low to high transition and remain high to be seen, but it will not be generated again until it makes another low to high transition.

SERIAL I/O

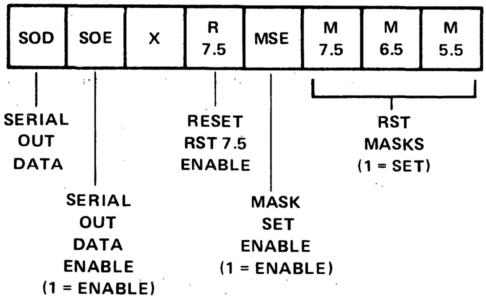
Serial input and output is accomplished with two new instructions not included in the 8080: RIM and SIM. These instructions serve several purposes: serial I/O, and reading or setting the interrupt mask.

The RIM (Read Interrupt Mask) instruction is used for reading the interrupt mask and for reading serial data. After execution of the RIM instruction the ACC content is as follows:



Note: After the TRAP interrupt, the RIM instruction must be executed to preserve the status of IE.

The SIM (Set Interrupt Mask) instruction is used to program the interrupt mask and to output serial data. Presetting the ACC for the SIM instruction has the following meaning:



INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also, the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the µPD8085A has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the µPD8085A. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the µPD8085A instruction set.

Two instructions, RIM and SIM, are used for reading and setting the internal interrupt mask as well as input and output to the serial I/O port.

The special instruction group completes the µPD8085A instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the µPD8085A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

TYPICAL INSTRUCTIONS

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Immediate mode or I/O instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND	

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Jump, call or direct load and store instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2	

INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2]								Clock Cycles[3]	FLAGS[4]			
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	4				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	4	●	●	●	
DCR d	Decrement register	0	0	d	d	d	1	0	1	4	●	●	●	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	●	●	●	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	●	●	●	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	●	●	●	●
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	●	●	●	●
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	●	●	●	●
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	●	●	●	●
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	●	●	●	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	●	●	●	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	●	●	●	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	●	●	●	●
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	●	●	●	●
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	●	●	●	●
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	●	●	●	●
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	●	●	●	●
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	●	●	●	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	●	●	●	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	●	●	●	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	●	●	●	●
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	●	●	●	●
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	●	●	●	●
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	●	●	●	●
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	●	●	●	●
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	●	●	●	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	●	●	●	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	●	●	●	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	●	●	●	●
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				●
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				●
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				●
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				●
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	7/10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	7/10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	7/10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	7/10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	7/10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	7/10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	7/10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	7/10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	18				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	9/18				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	9/18				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	9/18				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	9/18				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	9/18				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	9/18				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	9/18				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	9/18				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	6/12				
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12				
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12				
RC	Return on carry	1	1	0	1	1	0	0	0	6/12				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12				
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12				
RP	Return on positive	1	1	1	1	0	0	0	0	6/12				
RM	Return on minus	1	1	1	1	1	0	0	0	6/12				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2]								Clock Cycles[3]	FLAGS[4]			
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	12				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	12				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	12				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	●	●	●	●
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				●
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				●
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				●
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				●
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	6				
INX D	Increment DE	0	0	0	1	0	0	1	1	6				
INX H	Increment HL	0	0	1	0	0	0	1	1	6				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	6				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	6				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	6				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	6				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	6				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	16				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	6				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	6				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4				
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4				
RST.A	Restart	1	1	A	A	A	1	1	1	12				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				$\overline{Cy}$
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	●	●	●	●
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	5				

Notes

[1] Operand Symbols used

A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss 000 B · 001 C – 010 D – 011 E · 100 H
101 L – 110 Memory – 111 A

[3] Two possible cycle times (7/10) indicate instruction cycles dependent on condition flags.

[4] ● flag affected
flag not affected
0 - flag reset
1 flag set

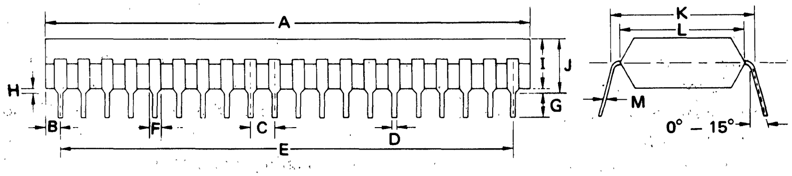
INSTRUCTION CYCLE TIMES

One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$).

Machine cycles and clock states used for each type of instruction are shown below.

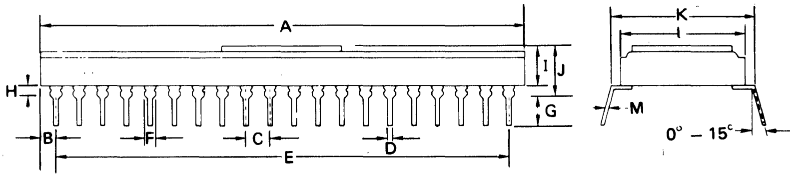
INSTRUCTION TYPE	MACHINE CYCLES EXECUTED MIN/MAX	CLOCK STATUS MIN/MAX
ALU R	1	4
CMC	1	4
CMA	1	4
DAA	1	4
DCR R	1	4
DI	1	4
EI	1	4
INR R	1	4
MOV R, R	1	4
NOP	1	4
ROTATE	1	4
RIM	1	4
SIM	1	4
STC	1	4
XCHG	1	4
HLT	1	5
DCX	1	6
INX	1	6
PCHL	1	6
RET COND.	1/3	6/12
SPHL	1	6
ALU I	2	7
ALU M	2	7
JNC	2/3	7/10
LDAX	2	7
MVI	2	7
MOV M, R	2	7
MOV R, M	2	7
STAX	2	7
CALL COND.	2/5	9/18
DAD	3	10
DCR M	3	10
IN	3	10
INR M	3	10
JMP	3	10
LOAD PAIR	3	10
MVI M	3	10
OUT	3	10
POP	3	10
RET	3	10
PUSH	3	12
RST	3	12
LDA	4	13
STA	4	13
LHLD	5	16
SHLD	5	16
XTHL	5	16
CALL	5	18

PACKAGE OUTLINE
μPD8085AC/D



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{\;0.05}$	$0.010^{+0.004}_{-0.002}$

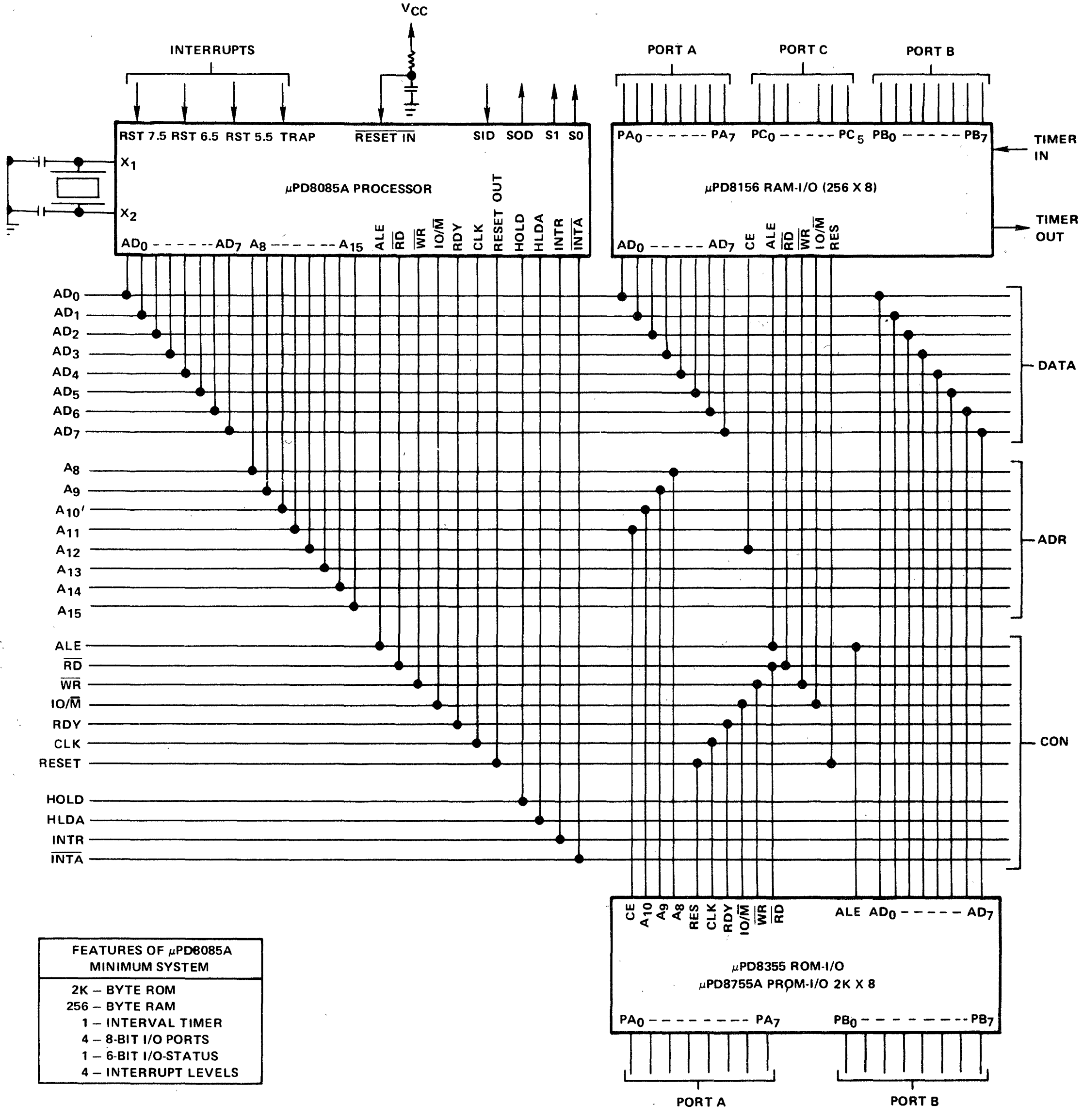


Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

μPD8085A FAMILY MINIMUM SYSTEM CONFIGURATION

A minimum computer system consisting of a processor, ROM, RAM, and I/O can be built with only 3-40 pin packs. This system is shown below with its address, data, control busses and I/O ports.



FEATURES OF μPD8085A MINIMUM SYSTEM

- 2K – BYTE ROM
- 256 – BYTE RAM
- 1 – INTERVAL TIMER
- 4 – 8-BIT I/O PORTS
- 1 – 6-BIT I/O-STATUS
- 4 – INTERRUPT LEVELS

NEC Microcomputers, Inc.

NEC
μPD8021

SINGLE CHIP 8-BIT MICROCOMPUTER

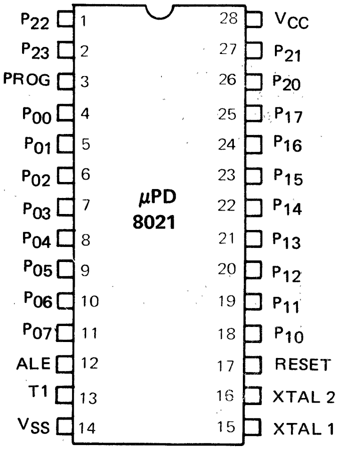
DESCRIPTION

The NEC μPD8021 is a stand alone 8-bit parallel microcomputer incorporating the following features usually found in external peripherals. The μPD8021 contains: 1K x 8 bits of mask ROM program memory, 64 x 8 bits of RAM data memory, 21 I/O lines, an 8-bit interval timer/event counter, and internal clock circuitry.

FEATURES

- 8-Bit Processor, ROM, RAM, I/O, Timer/Counter
- Single +5V Supply (+4.5V to +6.5V)
- NMOS Silicon Gate Technology
- 10 μs Cycle Time
- All Instructions 1 or 2 Cycles
- Instructions are Subset of μPD8048/8748/8035
- High Current Drive Capability – 2 I/O Pins
- Clock Generation Using Single Resistor or Inductor
- Zero-Cross Detection Capability
- Expandable I/O Using μPD8243's
- Available in 28 Pin Plastic Package

PIN CONFIGURATION



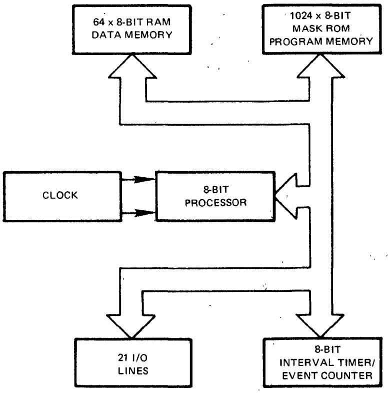
μPD8021

FUNCTIONAL DESCRIPTION

The NEC μPD8021 is a single component, 8-bit, parallel microprocessor using N-channel silicon gate MOS technology. The self-contained 1K x 8-bit ROM, 64 x 8-bit RAM, 8-bit timer/counter, and clock circuitry allow the μPD8021 to operate as a single-chip microcomputer in applications ranging from controllers to arithmetic processors.

The instruction set, a subset of the μPD8048/8748/8035, is optimum for high-volume, low cost applications where I/O flexibility and instruction set power are required. The μPD8021 instruction set is comprised mostly of single-byte instructions with no instructions over two bytes.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
(Plastic Package)	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1 Watt

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5.5V ± 1V; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		+ 0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IH}	2.0		V_{CC}	V	V_{CC} = 5.0V ± 10%
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	V_{CC} = 5.5V ± 1V
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (P_{10}, P_{11})	V_{OL1}			2.5	V	I_{OL} = 7 mA
Output High Voltage (All Unless Open Drain)	V_{OH}	2.4			V	I_{OH} = 50 μA
Output Leakage Current (Open Drain Option – Port 0)	I_{OL}			-10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
V_{CC} Supply Current	I_{CC}			60	mA	

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1-2, 26-27	P_{20}-P_{23} (Port 2)	P_{20}-P_{23} comprise the 4-bit bi-directional I/O port which is also used as the expander bus for the μPD8243.
3	PROG	PROG is the output strobe pin for the μPD8243.
4-11	P_{00}-P_{07} (Port 0)	One of the two 8-bit quasi bi-directional I/O ports.
12	ALE	Address Latch Enable output (active-high). Occurring once every 30 input clock periods, ALE can be used as an output clock.
13	T1	Testable input using transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction. T1 also provides zero-cross sensing for low-frequency AC input signals.
14	V_{SS}	Processor's ground potential.
15	XTAL 1	One side of frequency source input using resistor, inductor, crystal or external source. (non-TTL compatible V_{IH}).
16	XTAL 2	The other side of frequency source input.
17	RESET	RESET initializes the processor, setting program counter to zero and clearing status flip-flops.
18-25	P_{10}-P_{17} (Port 1)	The second of two 8-bit quasi bi-directional I/O ports.
28	V_{CC}	+5V power supply input.

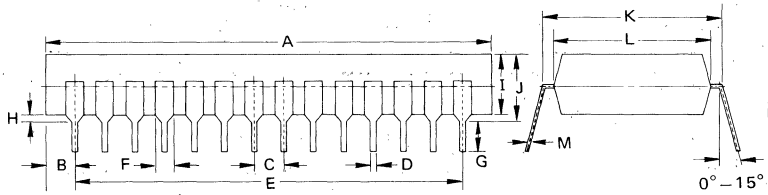
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5.5V ± 1V; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Cycle Time	T_{CY}	10.0		50.0	μs	3 MHz XTAL = 10 μs ①
Oscillator Frequency Variation (Resistor Mode)	Δ_F	−20		+20	%	F = 2.5 MHz ①

Note: ① Control outputs: C_L = 80 pF; R_L = 2.2K/4.3K

PACKAGE OUTLINE
μPD8021C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAG C
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
ACCUMULATOR													
ADD A, = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	●
Add A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	●
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	●
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	●
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	●
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	●
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1	
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1	
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1	
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1	
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	●
DEC A	(A) ← (A) - 1	DECREMENT by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1	
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1	
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1	
ORL A @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1	
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1	
RLC A	(AN + 1) ← (AN); N = 0 - 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	●
RR A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1	
RRC A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	●
SWAP A	($A_{4\text{-}7}$) ⇄ (A_0 - 3)	Swap the 24-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1	
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1	
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1	
BRANCH													
DJNZ Rr, addr	(Rr) ← (Rr) - 1; r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2	
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JMP addr	(PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
JMPP @ A	(PC 0 - 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1	
JNC addr	(PC 0 - 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNT1 addr	(PC 0 - 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JTF addr	(PC 0 - 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAG C
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
DATA MOVES													
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1	
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1	
MOV Rr, = data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2	
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1	
MOV @ Rr, A	((Rr)) ← (A); r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1	
MOV @ Rr, = data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2	
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1	
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1	
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1	
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1	
FLAGS													
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•
INPUT/OUTPUT													
ANLD Pp, A	(P_p) ← (P_p) AND (A 0 - 3) p = 4 - 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1	
IN A, P_p	(A) ← (P_p); p = 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1	
MOVD A, P_p	(A 0 - 3) ← (P_p); p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1	
MOVD P_p, A	(P_p) ← A 0 - 3; p = 4 - 7	Move contents of Accumulator to designated port (4 - 7).	0	0	1	1	1	1	p	p	1	1	
ORLD P_p, A	(P_p) ← (P_p) OR (A 0 - 3) p = 4 - 7	Logical or contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1	
OUTL P_p, A	(P_p) ← (A); p = 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1	
REGISTERS													
INC Rr	(Rr) ← (Rr) + 1; r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1	
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1	
SUBROUTINE													
CALL addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
RET	(SP) ← (SP) - 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1	
TIMER/COUNTER													
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1	
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1	
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1	
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1	
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1	
MISCELLANEOUS													
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1	

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions

SYMBOL	DESCRIPTION
A	The Accumulator
addr	Program Memory Address (12 bits)
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 - 7)
Rr	Register Designator (r = 0, 1 or 0 - 7)

SYMBOL	DESCRIPTION
T	Timer
T_1	Testable Flag 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

NEC

NEC Microcomputers, Inc.

μPD8041
μPD8741*

UNIVERSAL PROGRAMMABLE PERIPHERAL INTERFACE 8-BIT MICROCOMPUTERS

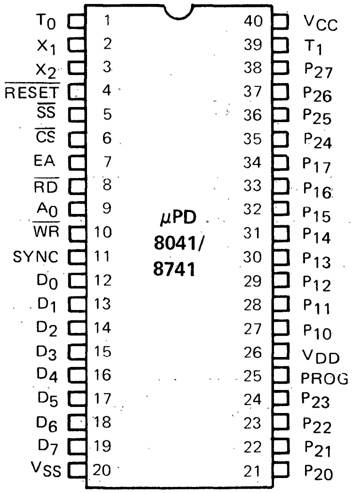
DESCRIPTION

The μPD8041 and μPD8741 are 8-bit single component microcomputers which function as general purpose programmable interfaces between the host processor and many various peripheral devices. The μPD8041 and μPD8741 differ only in their internal program memories. The μPD8041 contains 1024 x 8 bytes of mask ROM, while the μPD8741 contains 1024 x 8 bytes of UV EPROM. Some of the features offered by both devices include 64 x 8 bytes of RAM data memory, an 8-bit programmable counter/timer, 16 TTL compatible I/O lines, and two test inputs.

FEATURES

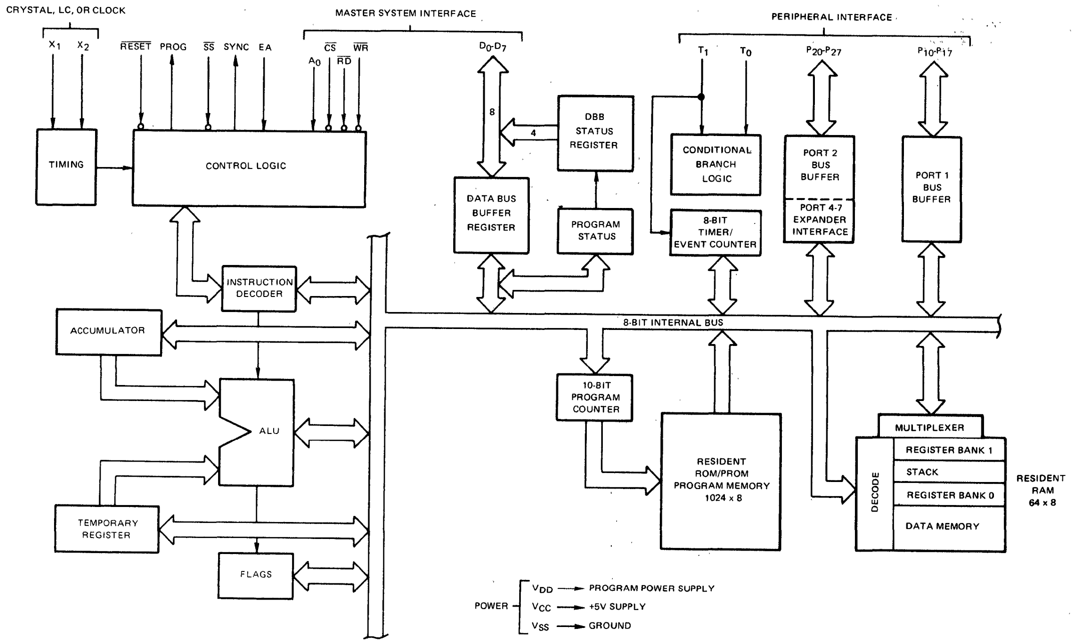
- Fully Compatible with 8080A, 8085A, and 8048 Families
- Single +5V Supply
- Fully Compatible ROM and EPROM Versions
- 1024 x 8 ROM/EPROM, 64 x 8 RAM
- 18 Programmable I/O Lines
- Expandable I/O
- Two Single Level Interrupts
- Single Package: 8-Bit Processor, ROM, RAM, Timer, I/O and Clock
- Asynchronous Data Register for Master Processor Interface
- Available in Both Plastic and Ceramic 40-Pin Packages

PIN CONFIGURATION



*All data pertaining to the μPD8741 is preliminary.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1.5 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: ① With respect to ground.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{DD} = V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage (All except X_1 and X_2)	V_{IL}	−0.5		+0.8	V	
Input High Voltage (All except X_1, X_2, $\overline{RESET}$)	V_{IH1}	2.0		V_{CC}	V	
Input High Voltage (X_1, X_2, $\overline{RESET}$)	V_{IH2}	3.0		V_{CC}	V	
Output Low Voltage (D_0-D_7, SYNC)	V_{OL1}			0.45	V	$I_{OL} = 2.0$ mA
Output Low Voltage (All other outputs except PROG)	V_{OL2}			0.45	V	$I_{OL} = 1.6$ mA
Output Low Voltage (PROG)	V_{OL3}			0.45	V	$I_{OL} = 1.0$ mA
Output High Voltage (D_0-D_7)	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
Output High Voltage (All other outputs)	V_{OH2}	2.4			V	$I_{OH} = -50\ \mu A$
Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0)	I_{IL}			±10	μA	$V_{SS} < V_{IN} < V_{CC}$
Output Leakage Current (D_0-D_7; High Z State)	I_{OL}			±10	μA	$V_{SS} + 0.45 < V_{IN} < V_{CC}$
V_{DD} Supply Current	I_{DD}			25	mA	
Total Supply Current	$I_{CC} + I_{DD}$			135	mA	
Low Input Source Current (P_{10}-P_{17}; P_{20}-P_{27})	I_{LI1}			0.4	mA	$V_{IL} = 0.8V$
Low Input Source Current (SS; $\overline{RESET}$)	I_{LI2}			0.2	mA	$V_{IL} = 0.8V$

PIN IDENTIFICATION

PIN		
NO.	SYMBOL	FUNCTION
1,39	T_0, T_1	Testable input pins using conditional transfer functions JT0, JNT0, JT1, JNT1. T_1 can be made the counter/timer input using the STRT CNT instruction. The PROM programming and verification on the 8741 uses T_0.
2	X_1	One side of the crystal input for external oscillator or frequency source.
3	X_2	The other side of the crystal input.
4	$\overline{\text{RESET}}$	Active-low input for processor initialization. $\overline{\text{RESET}}$ is also used for PROM programming, verification, and power down.
5	$\overline{\text{SS}}$	Single Step input (active-low). $\overline{\text{SS}}$ together with SYNC output allows the µPD8741 to "single-step" through each instruction in program memory.
6	$\overline{\text{CS}}$	Chip Select input (active-low). $\overline{\text{CS}}$ is used to select the appropriate µPD8041/8741 on a common data bus.
7	EA	External Access input (active-high). A logic "1" at this input commands the µPD8041/8741 to perform all program memory fetches from external memory.
8	$\overline{\text{RD}}$	Read strobe input (active-low). $\overline{\text{RD}}$ will pulse low when the master processor reads data and status words from the DATA BUS BUFFER or Status Register.
9	A_0	Address input which the master processor uses to indicate if a byte transfer is a command or data.
10	$\overline{\text{WR}}$	Write strobe input (active-low). $\overline{\text{WR}}$ will pulse low when the master processor writes data or status words to the DATA BUS BUFFER or Status Register.
11	SYNC	The SYNC output pulses once for each µPD8041/8741 instruction cycle. It can function as a strobe for external circuitry. SYNC can also be used together with $\overline{\text{SS}}$ to "single-step" through each instruction in program memory.
12-19	D_0-D_7 BUS	The 8-bit, bi-directional, tri-state DATA BUS BUFFER lines by which the µPD8041/8741 interfaces to the 8-bit master system data bus.
20	V_{SS}	Processor's ground potential.
21-24, 35-38	P_{20}-P_{27}	PORT 2 is the second of two 8-bit, quasi-bi-directional I/O ports. P_{20}-P_{23} contain the four most significant bits of the program counter during external memory fetches. P_{20}-P_{23} also serve as a 4-bit I/O bus for the µPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. PROG is used in programming the µPD8741. It is also used as an output strobe for the µPD8243.
26	V_{DD}	V_{DD} is the programming supply voltage for programming the µPD8741. It is +5V for normal operation of the µPD8041/8741. V_{DD} is also the Low Power Standby input for the ROM version.
27-34	P_{10}-P_{17}	PORT 1 is the first of two 8-bit quasi-bi-directional I/O ports.
40	V_{CC}	Primary power supply. V_{CC} must be +5V for programming and operation of the µPD8741 and for the operation of the µPD8041.

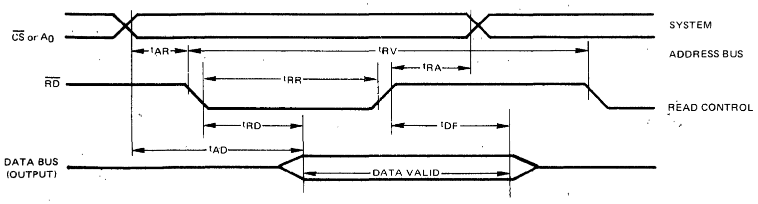
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{DD} = V_{CC} = +5V$; $V_{SS} = 0V$

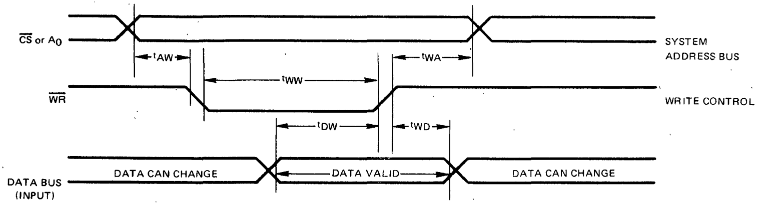
PARAMETER	SYMBOL	LIMITS				UNITS	TEST CONDITIONS
		μPD8041		μPD8741			
		MIN	MAX	MIN	MAX		
DBB READ							
$\overline{CS}$, A_0 Setup to $\overline{RD}$ ↓	t_{AR}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{RD}$ ↑	t_{RA}	0		30		ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		150		370	ns	
$\overline{RD}$ ↓ to Data Out Delay	t_{RD}		150		200	ns	
$\overline{RD}$ ↑ to Data Float Delay	t_{DF}	10		10		ns	
			100		140	ns	
Recovery Time between Reads and/or Writes	t_{RV}	1		1		μs	
Cycle Time	t_{CY}	2.5		2.5		μs	6 MHz Crystal
DBB WRITE							
$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	t_{AW}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{WR}$ ↑	t_{WA}	0		30		ns	
$\overline{WR}$ Pulse Width	t_{WW}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
Data Setup to $\overline{WR}$ ↑	t_{DW}	150		250		ns	
Data Hold after $\overline{WR}$ ↑	t_{WD}	0		30		ns	

TIMING WAVEFORMS

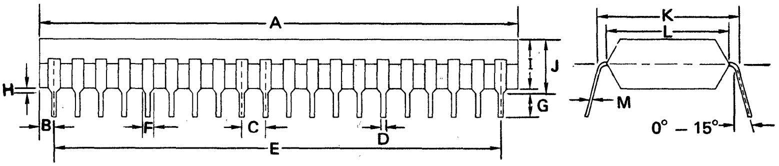
READ OPERATION — DATA BUS BUFFER REGISTER



WRITE OPERATION — DATA BUS BUFFER REGISTER

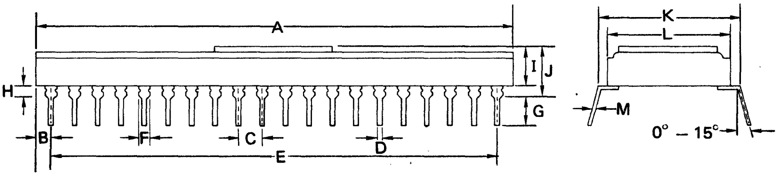


PACKAGE OUTLINE
μPD8041C/D
μPD8741C/D



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAGS					
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1	IBF	OBF
ACCUMULATOR																		
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	●					
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	●					
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	●					
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	●					
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	●					
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	●					
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1						
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1						
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1						
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1						
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	●					
DEC A	(A) ← (A) – 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1						
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1						
ORL A, = data	(A) ← (A) OR data	Logical OR or specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1						
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1						
RL A	(AN + 1) ← (AN) $(A_0) \leftarrow (A_7)$ for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1						
RLC A	(AN + 1) ← (AN); N = 0 – 6 $(A_0) \leftarrow (C)$ $(C) \leftarrow (A_7)$	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	●					
RR A	(AN) ← (AN + 1); N = 0 – 6 $(A_7) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1						
RRC A	(AN) ← (AN + 1); N = 0 – 6 $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	●					
SWAP A	$(A_{4\text{-}7}) \rightleftarrows (A_0 - 3)$	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1						
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1						
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1						
BRANCH																		
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2						
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2						
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JF0 addr	(PC 0 – 7) ← addr if FO = 1 (PC) ←)(PC) + 2 if FO = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2						
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1						
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JNIBF addr	(PC 0 – 7) ← addr if IBF = (PC) ← (PC) + 2 if IBF = 1	Jump to specified address if input buffer full flag is low.	1 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JOBF	(PC 0 – 7) ← addr if OBF = 1 (PC) ← (PC) + 2 if OBF = 0	Jump to specified address if output buffer full flag is set.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						

MNEMONIC	FUNCTION		INSTRUCTION CODE								CYCLES	BYTES	FLAGS					
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1	IBF	OBF
BRANCH (CONT.)																		
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a ⊥.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
CONTROL																		
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1						
DIS I		Disable the External Interrupt input	0	0	0	1	0	1	0	1	1	1						
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1						
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1						
DATA MOVES																		
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1						
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1						
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1						
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2						
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1						
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1						
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2						
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1						
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1						
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1						
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1						
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1						
XCHD A, @ Rr	(A 0 – 3) ⇆ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1						
FLAGS																		
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	●					
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			●			
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				●		
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	●					
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			●			
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				●		

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAGS					
			D7	D6	D5	D4	D3	D2	D1	D0			C	AC	F0	F1	IBF	OBF
INPUT/OUTPUT																		
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 - 2	Logical and Immediate specified data with designated port (1 or 2)	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 - 3) p = 4 · 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1						
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1						
IN A, DBB	(A) ← (DBB)	Input strobed DBB data into Accumulator and clear IBF	0	0	1	0	0	0	1	0	1	1					●	
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 · 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1						
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 - 7	Move contents of Accumulator to designated port (4 7).	0	0	1	1	1	1	p	p	1	1						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 7	Logical or contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1						
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 - 2	Logical or Immediate specified data with designated port (1 - 2)	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2						
OUT DBB, A	(DBB) (A)	Output contents of Accumulator onto DBB and set OBF.	0	0	0	0	0	0	1	0	1	1						●
OUTL Pp, A	(Pp) ← (A); p = 1 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1						
REGISTERS																		
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1						
INC Rr	(Rr) ← (Rr) +1; r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1						
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1						
SUBROUTINE																		
CALL addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2						
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1						
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1						
TIMER/COUNTER																		
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1						
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1						
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1						
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1						
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1						
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1						
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1						
MISCELLANEOUS																		
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1						

Notes ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.

② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

③ References to the address and data are specified in bytes 2 and or 1 of the instruction.

④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1.
I	Interrupt
P	"In-Page" Operation Designator
IBF	Input Buffer Full Flag

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By
OBF	Output Buffer Full
DBB	Data Bus Buffer

NEC Microcomputers, Inc.

NEC

μPD8048
μPD8748*
μPD8035

μPD8048 FAMILY OF SINGLE CHIP 8-BIT MICROCOMPUTERS

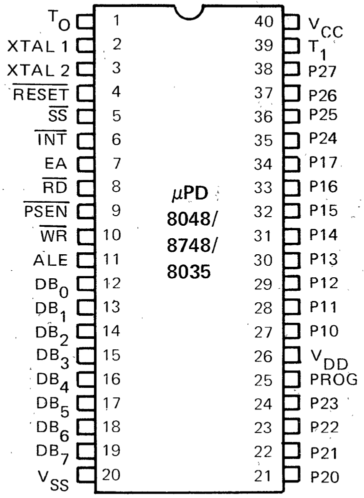
DESCRIPTION

The μPD8048 family of single chip 8-bit microcomputers is comprised of the μPD8048, μPD8748 and μPD8035. The processors in this family differ only in their internal program memory options: the μPD8048 with 1K x 8 bytes of mask ROM, the μPD8748 with 1K x 8 bytes of UV erasable EPROM and the μPD8035 with external memory.

FEATURES

- Fully Compatible With Industry Standard 8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 Byte RAM Data Memory
- Single Level Interrupt
- 96 Instructions: 70% Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages

PIN CONFIGURATION



*All data pertaining to the μPD8748 is preliminary.

FUNCTIONAL DESCRIPTION

The NEC µPD8048, µPD8748 and µPD8035 are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The µPD8048/8748/8035 efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The µPD8048/8748/8035 instruction set is comprised of 1 and 2 byte instructions with over 70% single-byte and requiring only 1 or 2 cycles per instruction with over 50% single-cycle.

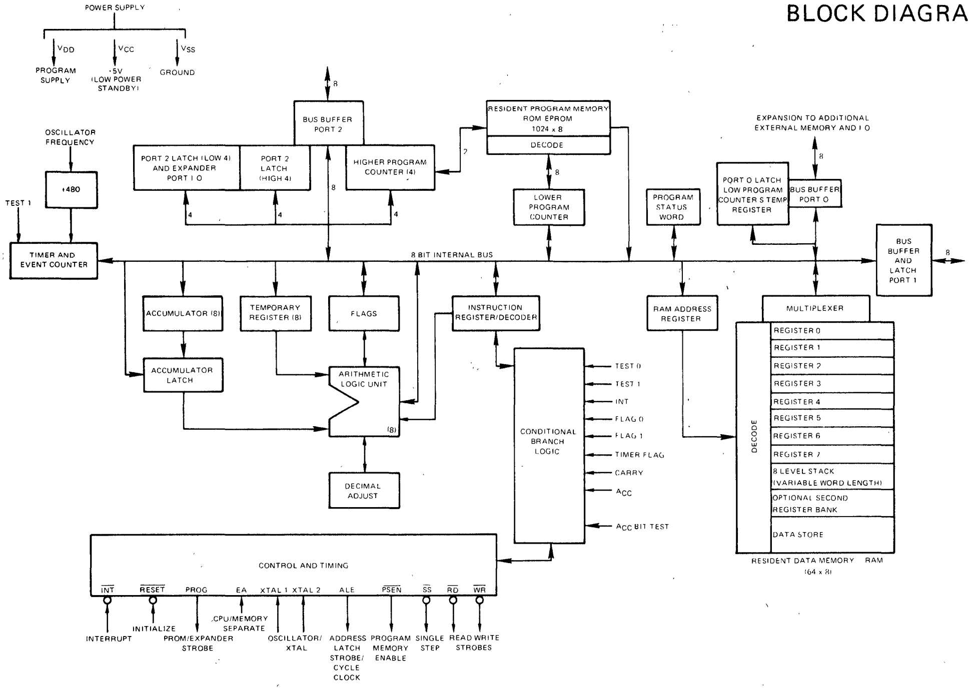
The µPD8048 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The µPD8048 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The µPD8748 differs from the µPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The µPD8035 is intended for applications using external program memory only. It contains all the features of the µPD8048 except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN		FUNCTION
NO.	SYMBOL	
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENT0 CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{\text{RESET}}$	Active low input for processor initialization. $\overline{\text{RESET}}$ is also used for PROM programming verification and power-down (non TTL compatible V_{IH}).
5	$\overline{\text{SS}}$	Single Step input (active-low). $\overline{\text{SS}}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{\text{INT}}$	Interrupt input (active-low). $\overline{\text{INT}}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{\text{INT}}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{\text{RD}}$	READ strobe output (active-low). $\overline{\text{RD}}$ will pulse low when the processor performs a BUS READ. $\overline{\text{RD}}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{\text{PSEN}}$	Program Store Enable output (active-low). $\overline{\text{PSEN}}$ becomes active only during an external memory fetch.
10	$\overline{\text{WR}}$	WRITE strobe output (active-low). $\overline{\text{WR}}$ will pulse low when the processor performs a BUS WRITE. $\overline{\text{WR}}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. PSEN controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{\text{RD}}$ and $\overline{\text{WR}}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21 – 24, 35 – 38	$P_{20} - P_{27}$: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27 – 34	$P_{10} - P_{17}$: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply. V_{CC} must be +5V for programming and operation of the μPD8748, and for operation of the μPD8035 and μPD8048.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	− 0.5 to +7 Volts ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$^*T_a = 25^\circ C$

DC CHARACTERISTICS

$T_a = 0^\circ C$ to $+70^\circ C$; $V_{CC} = V_{DD} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	
Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output Low Voltage (All Other Outputs Except PROG)	V_{OL1}			0.45	V	$I_{OL} = 1.6$ mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	
Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH}	2.4			V	$I_{OH} = -100\ \mu A$
Output High Voltage (All Other Outputs)	V_{OH1}	2.4			V	$I_{OH} = -50\ \mu A$
Input Leakage Current (T_1, EA, INT)	I_{IL}			±10	µA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
Output Leakage Current (BUS, T_0 – High Impedance State)	I_{OL}			10	µA	$V_{CC} \geqslant V_{IN} \geqslant V_{SS} + 0.45V$
Power Down Supply Current	I_{DD}		10	20	mA	$T_a = 25^\circ C$
Total Supply Current	$I_{DD} + I_{CC}$		65	135	mA	$T_a = 25^\circ C$

DC CHARACTERISTICS PROGRAMMING THE µPD8748

$T_a = 25^\circ C \pm 5^\circ C$; $V_{CC} = +5V \pm 5\%$; $V_{DD} = +25V \pm 1V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{DD} Program Voltage High-Level	V_{DDH}	24.0		26.0	V	
V_{DD} Voltage Low-Level	V_{DDL}	4.75		5.25	V	
PROG Voltage High-Level	V_{PH}	21.5		24.5	V	
PROG Voltage Low-Level	V_{PL}			0.2	V	
EA Program or Verify Voltage High-Level	V_{EAH}	21.5		24.5	V	
EA Voltage Low-Level	V_{EAL}			5.25	V	
V_{DD} High Voltage Supply Current	I_{DD}			30.0	mA	
PROG High Voltage Supply Current	I_{PROG}			16.0	mA	
EA High Voltage Supply Current	I_{EA}			1.0	mA	

AC CHARACTERISTICS

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

T_a = 0°C to +70°C; $V_{CC} = V_{DD}$ = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	150			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width ($\overline{\text{PSEN}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$)	t_{CC}	900			ns	
Data Setup before $\overline{\text{WR}}$	t_{DW}	500			ns	
Data Hold after $\overline{\text{WR}}$	t_{WD}	120			ns	C_L = 20 pF
Cycle Time	t_{CY}	2.5		15.0	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
$\overline{\text{PSEN}}$, $\overline{\text{RD}}$ to Data In	t_{RD}			500	ns	
Address Setup before $\overline{\text{WR}}$	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to $\overline{\text{RD}}$, $\overline{\text{PSEN}}$	t_{AFC}	0			ns	

Notes: ① For Control Outputs: C_L = 80 pF
② For Bus Outputs: C_L = 150 pF
③ t_{CY} = 2.5 μs

PORT 2 TIMING

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

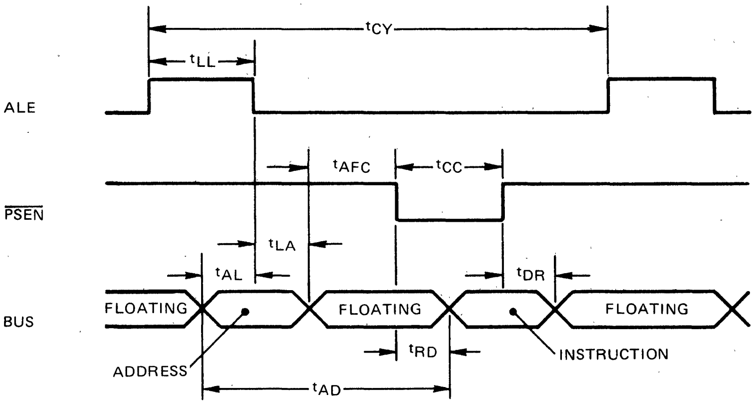
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Port Control Setup before Falling Edge of $\overline{\text{PROG}}$	t_{CP}	110			ns	
Port Control Hold after Falling Edge of $\overline{\text{PROG}}$	t_{PC}	140			ns	
$\overline{\text{PROG}}$ to Time P2 Input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	220			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}			150	ns	
$\overline{\text{PROG}}$ Pulse Width	t_{PP}	1510			ns	
Port 2 I/O Data Setup	t_{PL}	400			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

PROGRAMMING SPECIFICATIONS – μPD8748

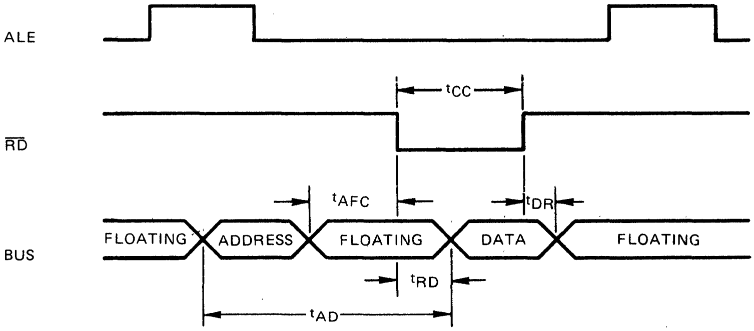
T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{DD} = +25V ± 1V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Setup Time before $\overline{\text{RESET}}$ ↑	t_{AW}	4 t_{CY}				
Address Hold Time after $\overline{\text{RESET}}$ ↑	t_{WA}	4 t_{CY}				
Data In Setup Time before $\overline{\text{PROG}}$ ↑	t_{DW}	4 t_{CY}				
Data In Hold Time after $\overline{\text{PROG}}$ ↓	t_{WD}	4 t_{CY}				
$\overline{\text{RESET}}$ Hold Time to VERIFY	t_{PH}	4 t_{CY}				
V_{DD}	t_{VDDW}	4 t_{CY}				
V_{DD} Hold Time after PROG ↓	t_{VDDH}	0				
Program Pulse Width	t_{PW}	50		60	ms	
Test 0 Setup Time before Program Mode	t_{TW}	4 t_{CY}				
Test 0 Hold Time after Program Mode	t_{WT}	4 t_{CY}				
Test 0 to Data Out Delay	t_{DO}			4 t_{CY}		
$\overline{\text{RESET}}$ Pulse Width to Latch Address	t_{WW}	4 t_{CY}				
V_{DD} and $\overline{\text{PROG}}$ Rise and Fall Times	t_r, t_f	0.5		2.0	μs	
Processor Operation Cycle Time	t_{CY}	5.0			μs	
$\overline{\text{RESET}}$ Setup Time before EA ↑	t_{RE}	4 t_{CY}				

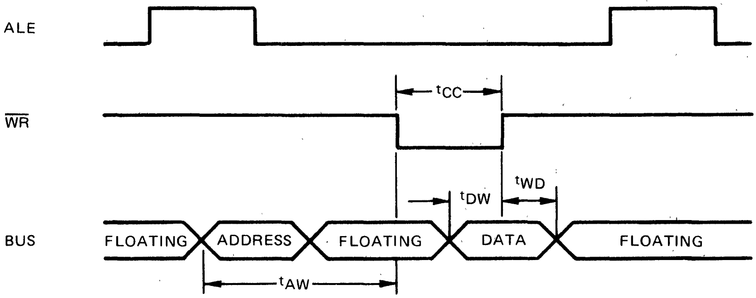
TIMING WAVEFORMS



INSTRUCTION FETCH FROM EXTERNAL MEMORY

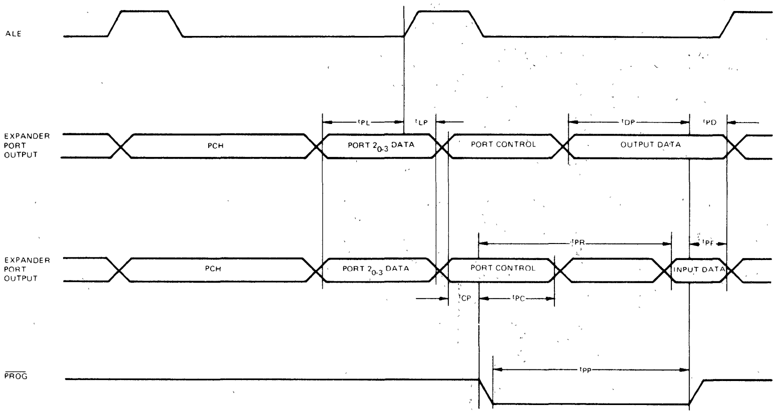


READ FROM EXTERNAL DATA MEMORY

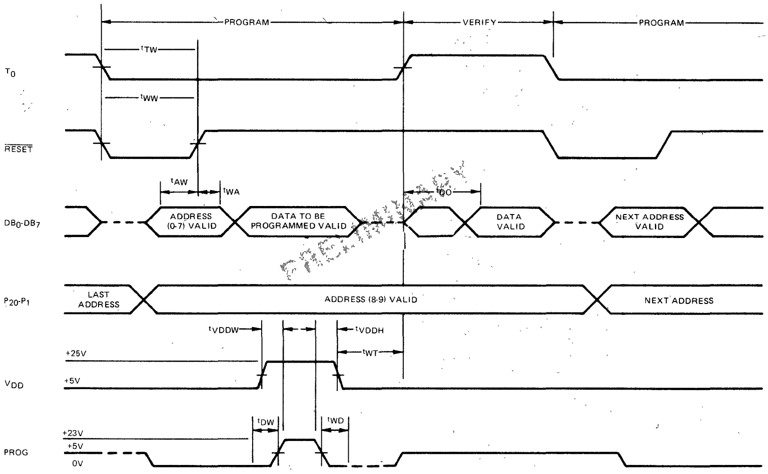


WRITE TO EXTERNAL MEMORY

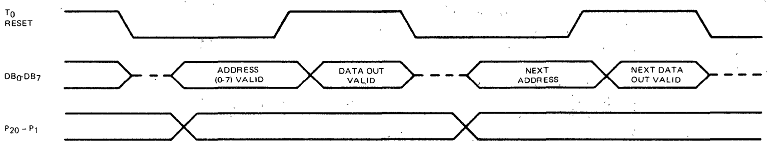
TIMING WAVEFORMS (CONT.)



PORT 2 TIMING



PROGRAM/VERIFY TIMING
(μPD8748 ONLY)



VERIFY MODE TIMING
(μPD8048/8748 ONLY)

Notes ① Conditions $\overline{CS}$ TTL Logic "1", Ao TTL Logic "0" must be met. (use 10K resistor to V_{CC} for $\overline{CS}$, and 10K resistor to V_{SS} for Ao)

② t_{CY} 5 μs can be achieved using a 3 MHz frequency source (LC, XTAL or external) at the XTAL 1 and XTAL 2 inputs.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAGS			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
ACCUMULATOR																
ADD A, # data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	●			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 − 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	●			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 − 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	●			
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	●			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 − 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	●			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 − 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	●			
ANL A, # data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 − 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 − 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	●			
DEC A	(A) ← (A) − 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 − 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 − 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) $(A_0) \leftarrow (A_7)$ for N = 0 − 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 − 6 $(A_0) \leftarrow (C)$ $(C) \leftarrow (A_7)$	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	●			
RR A	(AN) ← (AN + 1); N = 0 − 6 $(A_7) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 − 6 $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	●			
SWAP A	$(A_{4-7}) \rightleftarrows (A_0 - 3)$	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 − 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 − 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) − 1; r = 0 − 7 If (Rr) ≠ 0: (PC 0 − 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 − 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 − 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 − 7) ← addr if FO = 1 (PC) ← (PC) + 2 if FO = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 − 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 − 10) ← addr 8 − 10 (PC 0 − 7) ← addr 0 − 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 − 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 − 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 − 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAGS			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇆ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAGS			
			D7	D6	D5	D4	D3	D2	D1	D0			C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, # data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2)	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2)	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) – 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) +1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

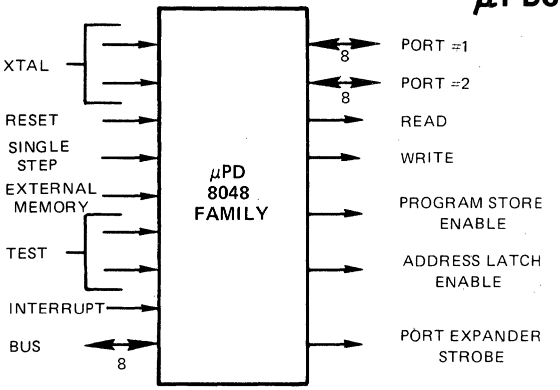
Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

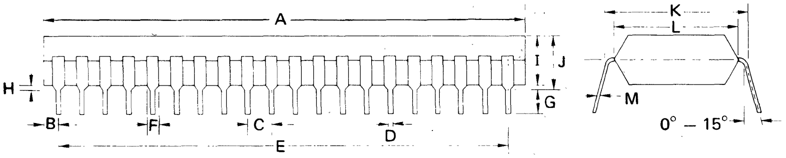
SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

LOGIC SYMBOL

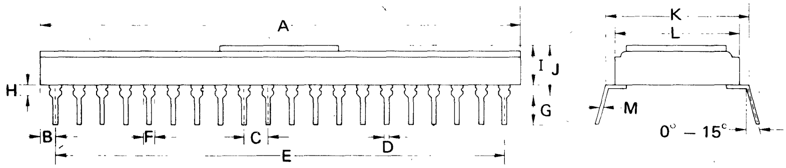


PACKAGE OUTLINES
μPD8048C/D
μPD8748D
μPD8035C/D



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

NEC Microcomputers, Inc.

NEC

µPD8049

µPD8039

PRELIMINARY

SINGLE CHIP 8-BIT MICROCOMPUTERS

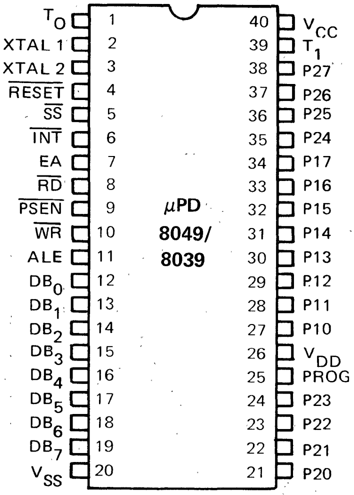
DESCRIPTION

The NEC µPD8049 and µPD8039 are single chip 8-bit microcomputers. The processors differ only in their internal program memory options: the µPD8049 with 2K x 8 bytes of mask ROM and the µPD8039 with external program memory.

FEATURES

- Fully Compatible with Industry Standard 8049/8039
- Pin Compatible with the µPD8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 µs Cycle Time. All Instructions 1 or 2 Bytes
- Interval Timer/Event Counter
- 2K x 8 Bytes of ROM, 128 x 8 Bytes of RAM
- Single Level Interrupt
- 96 Instructions: 70 Percent Single Byte
- 27 I/O Lines
- Internal Clock Generator
- Compatible with 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40-Pin Packages

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The NEC μPD8049 and μPD8039 are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8049 and μPD8039 efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

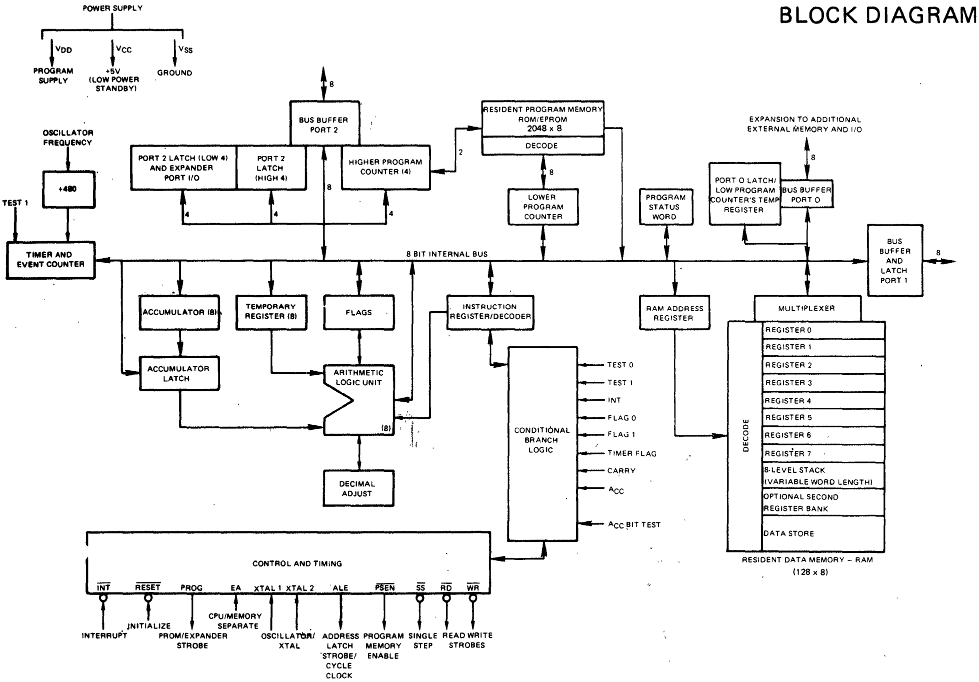
The μPD8049 and μPD8039 instruction set is comprised of 1 and 2 byte instructions with over 70 percent single-byte and requiring only 1 or 2 cycles per instruction with over 50 percent single-cycle.

The μPD8049 and μPD8039 microprocessors will function as stand-alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8049 contains the following functions usually found in external peripheral devices: 2048 x 8 bits of mask ROM program memory; 128 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; and oscillator and clock circuitry.

The μPD8039 is intended for applications using external program memory only. It contains all the features of the μPD8049 except the 2048 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN		FUNCTION
NO.	SYMBOL	
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. PSEN controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21 – 24, 35 – 38	$P_{20} - P_{27}$: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is the output strobe for the μPD8243 I/O expander.
26	V_{DD}	V_{DD} is +5V for normal operation. It also functions as low power standby pin.
27 – 34	$P_{10} - P_{17}$: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V during normal operation.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	− 0.5 to +7 Volts ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

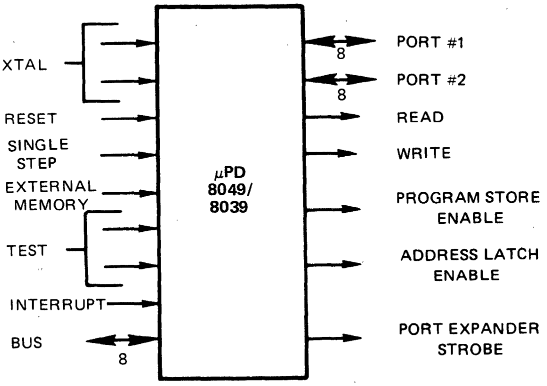
$^*T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage ($\overline{RESET}$, XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	
Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output Low Voltage (All Other Outputs Except PROG)	V_{OL1}			0.45	V	$I_{OL} = 1.6$ mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	
Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH}	2.4			V	$I_{OH} = -100\,\mu A$
Output High Voltage (All Other Outputs)	V_{OH1}	2.4			V	$I_{OH} = -50\,\mu A$
Input Leakage Current (T_1, EA, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (BUS, T_0 – High Impedance State)	I_{OL}			-10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$
Power Down Supply Current	I_{DD}		20	50	mA	$T_a = 25°C$
Total Supply Current	$I_{DD} + I_{CC}$		75	140	mA	$T_a = 25°C$

LOGIC SYMBOL



AC CHARACTERISTICS

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

$T_a = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	150			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width ($\overline{\text{PSEN}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$)	t_{CC}	900			ns	
Data Setup before $\overline{\text{WR}}$	t_{DW}	500			ns	
Data Hold after $\overline{\text{WR}}$	t_{WD}	120			ns	$C_L = 20$ pF
Cycle Time	t_{CY}	2.5		15.0	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
$\overline{\text{PSEN}}$, $\overline{\text{RD}}$ to Data In	t_{RD}			500	ns	
Address Setup before $\overline{\text{WR}}$	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to $\overline{\text{RD}}$, $\overline{\text{PSEN}}$	t_{AFC}	0			ns	

Notes: ① For Control Outputs: $C_L = 80$ pF

② For Bus Outputs: $C_L = 150$ pF

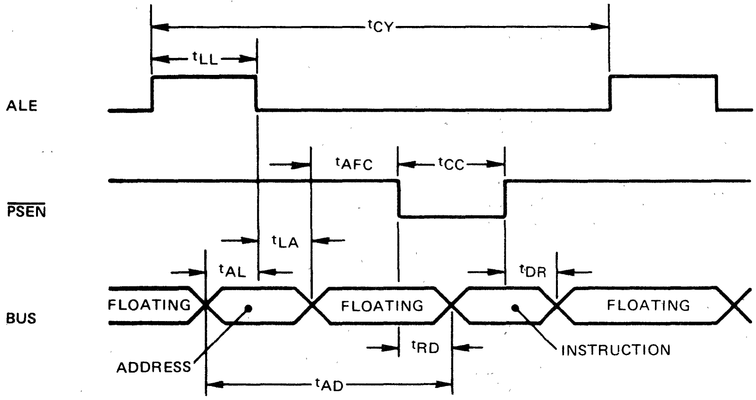
③ $t_{CY} = 2.5$ μs

PORT 2 TIMING

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

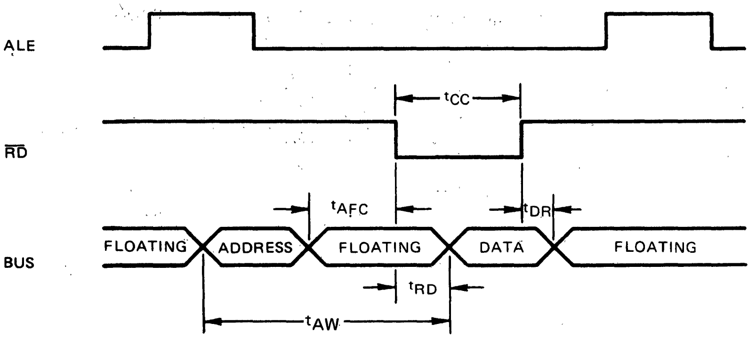
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of PROG	t_{CP}	110			ns	
Port Control Hold after Falling Edge of PROG	t_{PC}	140			ns	
PROG to Time P2 Input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	220			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}	0		150	ns	
PROG Pulse Width	t_{PP}	1510			ns	
Port 2 I/O Data Setup	t_{PL}	400			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

TIMING WAVEFORMS

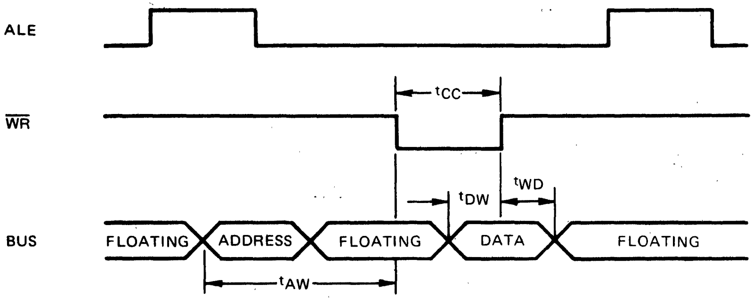


INSTRUCTION FETCH FROM EXTERNAL MEMORY

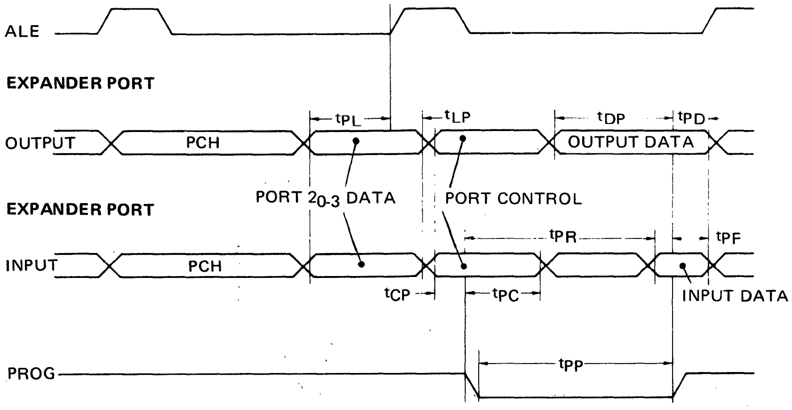
TIMING WAVEFORMS (CONT.)



READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL MEMORY



PORT 2 TIMING

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAGS			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
ACCUMULATOR																
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	●			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	●			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	●			
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	●			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator	0	1	1	1	1	r	r	r	1	1	●			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	●			
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	●			
DEC A	(A) ← (A) – 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) $(A_0) \leftarrow (A_7)$ for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 – 6 $(A_0) \leftarrow (C)$ $(C) \leftarrow (A_7)$	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	●			
RR A	(AN) ← (AN + 1); N = 0 – 6 $(A_7) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	●			
SWAP A	$(A_{4-7}) \leftrightarrows (A_{0-3})$	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr if FO = 1 (PC) ←)(PC) + 2 if FO = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES	FLAGS			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, = data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, = data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇆ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	●			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			●	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				●
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	●			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			●	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				●

MNEMONIC	FUNCTION	DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	C	AC	F0	F1
			INSTRUCTION CODE										FLAGS			
INPUT/OUTPUT																
ANL BUS, # data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2)	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2)	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) - 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) +1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.

② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.

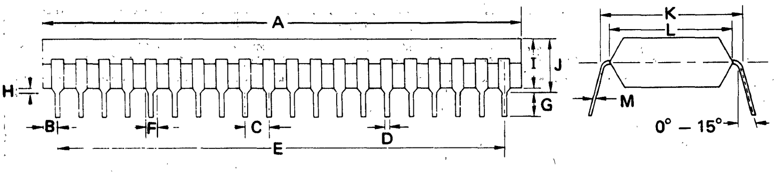
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

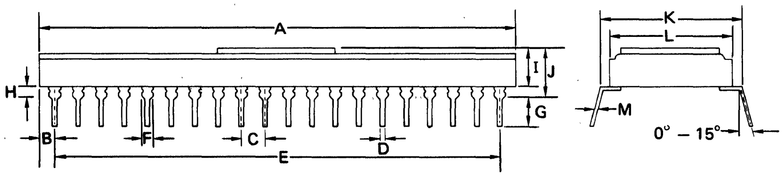
SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

PACKAGE OUTLINES
μPD8049C/D
μPD8039C/D



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

NEC Microcomputers, Inc.

NEC
μPD371

MAGNETIC TAPE CASSETTE/CARTRIDGE CONTROLLER

DESCRIPTION

The NEC μPD371 is a high performance N-Channel LSI tape cassette/cartridge controller designed to interface between most cassette or cartridge tape drives and most microprocessors or minicomputers.

The μPD371 converts 8-bit parallel data into serial phase encoded data to be written on tape and converts phase encoded data read from tape into 8-bit parallel data, calculates the CRC during write operations, verifies the CRC during read operations, informs the processor program when to send data bytes during write operations and when to read bytes during read operations, converts tape drive status signals into register bit levels which may be read by the processor program and converts software commands into signals which may be understood by the tape drive(s).

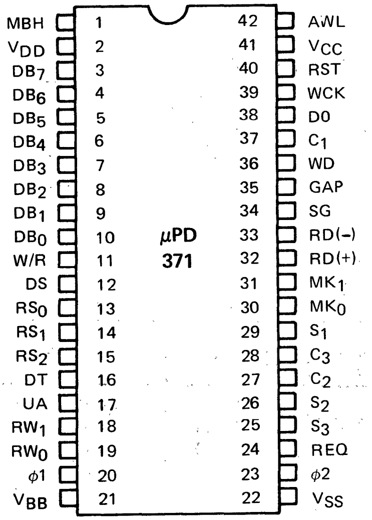
The μPD371 read and write data paths are completely separate to allow read-after-write data verification.

The μPD371 places no limitation on the selection of tape speed since the μPD371 maximum data transfer rate is considerably faster than that of the fastest cassette or cartridge drive.

FEATURES

- Compatible with ANSI, ECMA and ISO standard
- Also compatible with most other standards
- Hardware CRC generation and verification
- Read-after-write capability
- High speed file search
- Multiple drive capability
- May read or write on one drive while rewinding or file searching on another
- Maximum Data Transfer rate of 375K bits/sec equivalent to 468 IPS at 800 BPI

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−1 to +8 Volts ①
All Input Voltages	−1 to +8 Volts ①
Clock Voltages	−1 to +16 Volts ①
Supply Voltage V_{DD}	−1 to +16 Volts ①
Supply Voltage V_{CC}	−1 to +8 Volts ①
Supply Voltage V_{BB}	−10 to 0 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

Note: ① $V_{BB} = -5V \pm 5\%$. All voltages measured with respect to GND.

DC CHARACTERISTICS

$T_a = 0 - 70°C$ $V_{DD} = +12V \pm 5\%$ $V_{CC} = +5V \pm 5\%$ $V_{BB} = -5V \pm 5\%$ $V_{SS} = 0V$

PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP	MAX		
Input High Voltage		V_{IH}	+3.0		V_{CC}	V	
Input Low Voltage		V_{IL}	0		+0.8	V	
Output High Voltage		V_{OH}	+3.5			V	$I_{OH} = -1$ mA
Output Low Voltage		V_{OL}			+0.4	V	$I_{OL} = +1.7$ mA
Clock Input High Voltage		V_{OH}	+9		V_{DD}	V	
Clock Input Low Voltage		V_{OL}	0		+0.65	V	
Input Leakage Current		I_{LIH}			+10	μA	$V_I = +3.0V$
Input Leakage Current	$DB_0 - DB_7$	$I_{LIL\ 1}$			−10	μA	$V_I = +0.8V$
	All Except $DB_0 - DB_7$ (~25K Internal Pull-ups)	$I_{LIL\ 2}$			−1.0	mA	$V_I = +0.4V$
Clock Input Leakage Current		I_{LOH}			+20	μA	$V_O = +9.0V$
Clock Input Leakage Current		I_{LOL}			−20	μA	$V_O = +0.65V$
Output Leakage Current		I_{LOH}			+10	μA	$V_O = +3.5V$
Output Leakage Current		I_{LOL}			−10	μA	$V_O = +0.4V$
Power Supply Current (V_{DD})		I_{DD}		+20		mA	
Power Supply Current (V_{CC})		I_{CC}		+30		mA	
Power Supply Current (V_{BB})		I_{BB}			−2	mA	

CAPACITANCE

$T_a = 25°C$, $V_{DD} = V_{CC} = V_{SS} = 0V$, $V_{BB} = -5V$

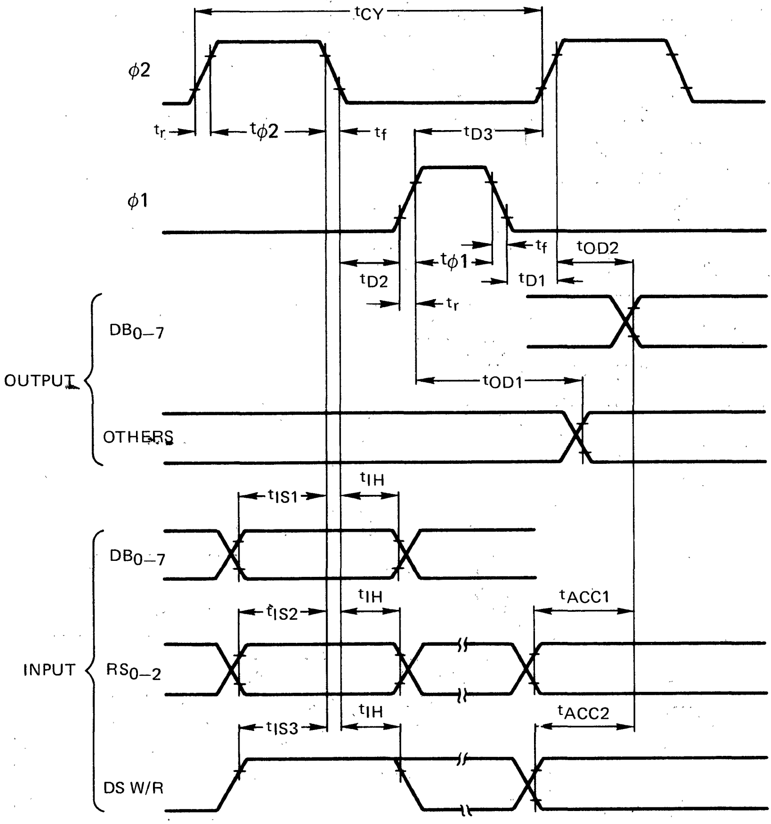
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Capacitance	C_O			35	pF	fc = 1 MHz. All pins except measuring pin are grounded.
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

AC CHARACTERISTICS

T_a = 0 – 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = CU

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{cy}	480		5000	ns	
Clock Rise and Fall Times	t_r, t_f	0		50	ns	
φ1 Pulse Width	$t_{\phi 1}$	60			ns	
φ2 Pulse Width	$t_{\phi 2}$	220			ns	
φ1 to φ2 Delay	t_{D1}	0			ns	
φ2 to φ1 Delay	t_{D2}	70			ns	
Delay φ1 to φ2 Lead Edges	t_{D3}	80			ns	
Data Out Delay from φ1	t_{OD1}			480	ns	1TTL & CL = 30 pF
Data Out Delay from φ1	t_{OD2}			260	ns	1TTL & CL = 30 pF
RS_0 – RS_2 to Output Delay	t_{ACC1}			300	ns	1TTL & CL = 30 pF
DS, W/R to Output Delay	t_{ACC2}			200	ns	1TTL & CL = 30 pF
DB_0 – DB_7 to φ2 Setup Time	t_{IS1}	250			ns	
RS_0 – RS_2 to φ2 Setup Time	t_{IS2}	350			ns	
DS, W/R to φ2 Setup Time	t_{IS3}	150			ns	
Input Hold Time from φ2	t_{IH}	30			ns	

TIMING WAVEFORMS



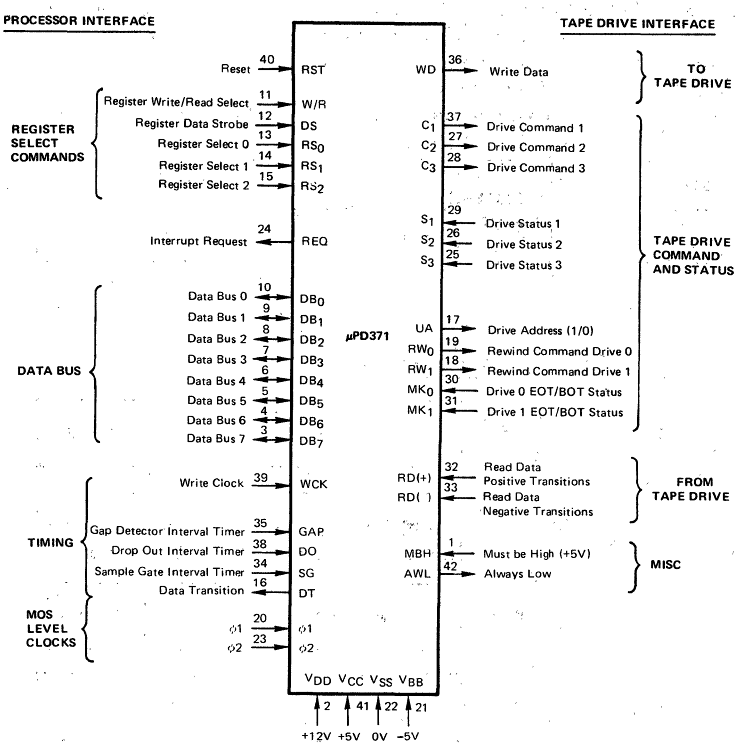
Note: Timing Measurement Levels:
Clock High/Low Voltage = 9.0V/0.65V
Input High/Low Voltage = 3.0V/0.8V
Output High/Low Voltage = 2.0V/0.8V

PIN IDENTIFICATION①

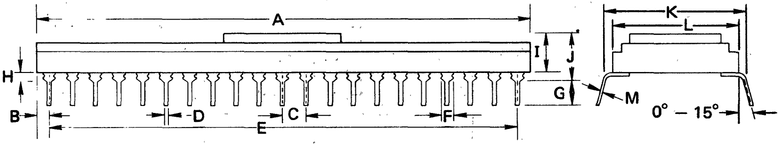
PIN			FUNCTION
NO.	SYMBOL	NAME	
RESET			
40	RST	Reset	A logic one at this pin causes a general reset of the µPD371.
REGISTER SELECT COMMANDS AND DATA BUS			
11	W/R		W/R, DS and $RS_0 - RS_2$ control Data Bus transfers between the µPD371 and the processor as follows: Writing into a µPD371 register: When W/R is a logic one, information the processor places on $DB_0 - DB_7$ is written into the µPD371 WRITE REGISTER selected by $RS_0 - RS_2$. The information is strobed into the register by a logic one at DS. Reading from a µPD371 register: When W/R is a logic zero, information from the µPD371 READ REGISTER selected by $RS_0 - RS_2$ is placed on $DB_0 - DB_7$ to be read by the processor. The information remains on $DB_0 - DB_7$ as long as DS is a logic one.
12	DS		
13 – 15	$RS_0 - RS_2$		
3 – 10	$DB_0 - DB_7$	Data Bus	
INTERRUPT REQUEST			
24	REQ		The µPD371 may be operated with either interrupt or polling techniques. If the interrupt technique is chosen, REQ should be connected to the interrupt request input of the processor. There are three sources of interrupt: READ BUFFER FULL, WRITE BUFFER EMPTY and GAP DETECTION.
TIMING			The user must provide four timing signals to the µPD371 – one for write operations and three for read operations. Each is defined in terms of T, where T is the period between successive data transitions in the phase encoded data written onto or read from tape.
39	WCK		WCK determines the WRITE DATA (WD, pin 36) transfer rate. WCK should have a period of 0.5T. DT is a pulse provided by the µPD371 to be used in the generation of the three read timing signals – SG, DO, and GAP. DT occurs at each data transition in the data read from tape. The internal read data sample gate is closed following each data transition and is reopened by a positive transition at SG 0.75T µsec after each DT pulse. A positive transition should be made at DO whenever a DT pulse stream ceases for a period of 1.5T µsec. A positive transition should be made at GAP whenever a DT pulse stream ceases for a period of 4T µsec. $\phi 1$ and $\phi 2$ are MOS level (12V) clock pulses. The timing of $\phi 1$ and $\phi 2$ is shown in the Timing Diagram.
16	DT		
34	SG		
38	DO		
35	GAP		
20	$\phi 1$		
23	$\phi 2$		
WRITE DATA			
36	WD		Phase encoded data to be written on tape leaves the µPD371 at pin 36.
TAPE DRIVE COMMAND AND STATUS			
37	C_1		C_1, C_2 and C_3 are general purpose tape drive commands. C_1, C_2 and C_3 are set and reset by the software manipulation of bits 5, 6 and 7, respectively, in Write Register 3. Since C_1, C_2 and C_3 are defined by software, they may be configured for any purpose. Typical uses for C_1, C_2 and C_3 are WRITE ENABLE, FORWARD and REVERSE.
27	C_2		
28	C_3		
29	S_1		S_1, S_2 and S_3 are general purpose tape drive status inputs. Their logic levels are indicated by bits 3, 4 and 7 of Read Register 1, respectively. Typical tape drive status signals are WRITE PERMIT, CASSETTE IN PLACE and SIDE. The µPD371 can adapt to any tape drive status signal set with a slight change in software.
26	S_2		
25	S_3		
DUAL TAPE DRIVE SYSTEM COMMAND AND STATUS			
17	UA	Unit Address	Selects Drive 0 when low and Drive 1 when high.
19	RW_0	Rewind 0	Rewind Command for Drive 0.
18	RW_1	Rewind 1	Rewind Command for Drive 1.
30	MK_0	Marker 0	EOT/BOT status from Drive 0.
31	MK_1	Marker 1	EOT/BOT status from Drive 1.
READ DATA			
32	RD(+)	Read Data (+)	A positive pulse from the tape drive at each positive transition in the read data.
33	RD(–)	Read Data (–)	A positive pulse from the tape drive at each negative transition in the read data.
MISCELLANEOUS			
1	MBH		MBH must be tied to the V_{CC} (+5V) supply.
42	AWL		AWL is a logic low output under all normal operating conditions of the µPD371.
POWER SUPPLY VOLTAGES			
2	V_{DD}		+12V
41	V_{CC}		+5V
22	V_{SS}		Ground
21	V_{BB}		–5V

Note: ① Refer to diagram on following page.

PIN IDENTIFICATION (CONT.)



PACKAGE OUTLINE μPD371D



ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

ADDRESSABLE INTERNAL REGISTERS

From the point of view of the processor program, the µPD371 makes the tape drive (or multiple drive system) appear as ten addressable registers. The program controls the drive(s) and transmits data to be written on tape by manipulating bits in the six µPD371 Write Registers. The program senses the status of the drive(s) and reads data stored on tape by reading bits from the four µPD371 Read Registers.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS_2	RS_1	RS_0		7	6	5	4	3	2	1	0
				WRITE REGISTERS								
1	0	0	0	WR_0	RST	MBL	SRS	WME	WCR	X	WMD	GNT
1	0	0	1	WR_1	WRR	RRR	X	RRE	RRD	GRE	GRD	X
1	0	1	0	WR_2	WD_7	WD_6	WD_5	WD_4	WD_3	WD_2	WD_1	WD_0
1	0	1	1	WR_3	C_3	C_2	C_1	RRI	RW	X	X	X
1	1	0	1	WR_5	X	X	X	RME	RMD	X	X	X
1	1	1	0	WR_6	X	X	X	X	X	X	X	UA
				READ REGISTERS								
0	0	0	0	RR_0	AWH	AWL	C_2	C_3	RDF	GRQ	WRQ	RRQ
0	0	0	1	RR_1	S_3	MK	MKF	S_2	S_1	RW	C_1	UA
0	0	1	0	RR_2	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0
0	0	1	1	RR_3	WD	GPF	REC	CRE	DOE	COR	NBR	NAR

X = NOT USED

ADDRESSABLE INTERNAL REGISTER BIT IDENTIFICATION

BIT	SYMBOL	NAME
WRITE REGISTER 0		
0	GNT	Gap Noise Tolerance
1	WMD	Write Mode Disable
2	–	Not used
3	WCR	Write CRC
4	WME	Write Mode Enable
5	SRS	Status Reset
6	MBL	Must Be Low
7	RST	Reset
WRITE REGISTER 1		
0	–	Not used
1	GRD	Gap Request Disable
2	GRE	Gap Request Enable
3	RRD	Read Request Disable
4	RRE	Read Request Enable
5	–	Not used
6	RRR	Read Request Reset
7	WRR	Write Request Reset
WRITE REGISTER 2		
0 – 7	WD_0 – WD_7	Write Buffer Register
WRITE REGISTER 3		
0	–	Not used
1	–	Not used
2	–	Not used
3	RW	Rewind
4	RRI	Rewind Reset Inhibit
5	C_1	Command One
6	C_2	Command Two
7	C_3	Command Three
WRITE REGISTER 4		
–	–	Not used
WRITE REGISTER 5		
0	–	Not used
1	–	Not used
2	–	Not used
3	RMD	Read Mode Disable
4	RME	Read Mode Enable
5	–	Not used
6	–	Not used
7	–	Not used

BIT	SYMBOL	NAME
WRITE REGISTER 6		
0	UA	Unit Address
1 – 7	–	Not used
READ REGISTER 0		
0	RRQ	Read Request
1	WRQ	Write Request
2	GRQ	Gap Request
3	RDF	Read Flag
4	C_3	Command 3
5	C_2	Command 2
6	AWL	Always Low
7	AWH	Always High
READ REGISTER 1		
0	UA	Unit Address
1	C_1	Command 1
2	RW	Rewind
3	S_1	Status 1
4	S_2	Status 2
5	MKF	Marker Flag
6	MK	Marker
7	S_3	Status 3
READ REGISTER 2		
0 – 7	RD_0 – RD_7	Read Buffer Register
READ REGISTER 3		
0	NAR	Noise After Record
1	NBR	Noise Before Record
2	COR	Command Overrun
3	DOE	Drop Out Error
4	CRE	CRC Error
5	REC	Record Detection
6	GPF	Gap Flag
7	WD	Write Data

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μPD372

FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD372D is a single LSI floppy disk controller chip which contains the circuitry to read, write, track seek, load and unload the head, generate and detect CRC characters, and perform all other floppy disk operations. It is completely compatible with the IBM, Minifloppy*TM, hard sector, and other formats and controls up to 4 floppy disk drives. The μPD372D may be interfaced directly to a host processor; or to a controller processor first, which in turn is interfaced to the host. These processors do not necessarily have to be of the 8080A type.

Data transfers to and from the μPD372D are done through addressable internal registers. These internal regsiters allow a large variety of system architectures to be configured; they provide status information on the drive, as well as perform data transfers between the drive and the processor.

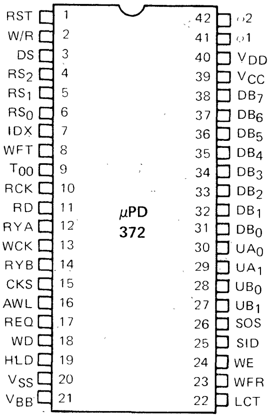
The μPD372D issues interrupts to the processor upon detection of an address mark and then when each subsequent data byte is available during either reading or writing. An 8-bit bi-directional data bus and 5 register select lines provide access to the 9 internal registers' contents. An internal interval timer is provided which facilitates performing such drive timing functions as: stepping rate, head settling time, track settling time, etc.

*TMShugart Associates.

FEATURES

- Compatible with IBM 3740 format
- Also compatible with other formats including Minifloppy and hard sector
- Controls up to four floppy disk drives
- Can perform overlap seeks
- Input and output TTL compatible (except for $\phi 1$ and $\phi 2$)
- Interfaces to most microprocessors including 8080A
- Standard power supplies (+12V, +5V and –5V)
- Controls most floppy disk drives including:
  - CALCOMP 140, 142
  - CDC BR803
  - INNOVEX 210, 410
  - PERTEC FD400
  - POTTER DD4740
  - SHUGART SA900, SA800
  - GSI 110
  - ORBIS 74, 76/77
  - PERSCI 70, 75
  - REMEX RFS 7400
  - SHUGART SA400 (Minifloppy)
  - WANGCO 82 (Minifloppy)
  - GSI MDD50 (Minifloppy)

PIN CONFIGURATION



Rev/2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−1.0 to +8 Volts①
All Input Voltages	−1.0 to +8 Volts①
Clock Voltage	−1.0 to +16 Volts①
Supply Voltage V_{DD}	−1.0 to +16 Volts①
Supply Voltage V_{CC}	−1.0 to +8 Volts①
Supply Voltage V_{BB}	−10 to +0 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

Note: ① $V_{BB} = -5V \pm 5\%$

DC CHARACTERISTICS

$T_a = -70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH}	+3.0		V_{CC}	V	
Low Level Input Voltage	V_{IL}	0		+0.8	V	
High Level Output Voltage	V_{OH}	+3.5			V	$I_{OH} = -1.0$ mA
Low Level Output Voltage	V_{OL1}①			+0.5	V	$I_{OL} = +1.7$ mA
	V_{OL2}②			+0.5	V	$I_{OL} = +3.3$ mA
High Level Clock Voltage	$V_{\phi H}$	+9		V_{DD}	V	
Low Level Clock Voltage	$V_{\phi L}$	0		+0.8	V	
High Level Input Leakage Current	I_{LIH}			+10	μA	$V_I = +3.0V$
Low Level Input Leakage Current	I_{LIL}			−10	μA	$V_I = +0.8V$
High Level Clock Leakage Current	$I_{L\phi H}$			+10	μA	$V_\phi = +9.0V$
Low Level Clock Leakage Current	$I_{L\phi L}$			−10	μA	$V_\phi = +0.8V$
High Level Output Leakage Current	I_{LOH}			+10	μA	$V_O = +3.5V$
Low Level Output Leakage Current	I_{LOL}			−10	μA	$V_O = +0.5V$
Power Supply Current (V_{DD})	I_{DD}		+20		mA	
Power Supply Current (V_{CC})	I_{CC}		+23		mA	
Power Supply Current (V_{BB})	I_{BB}			−2	mA	

Notes: ① CKS, REQ, UA_0, UA_1, UB_0, UB_1, DB_0–DB_7.

② WD, HLD, LCT, WE, WFR, SOS, SID.

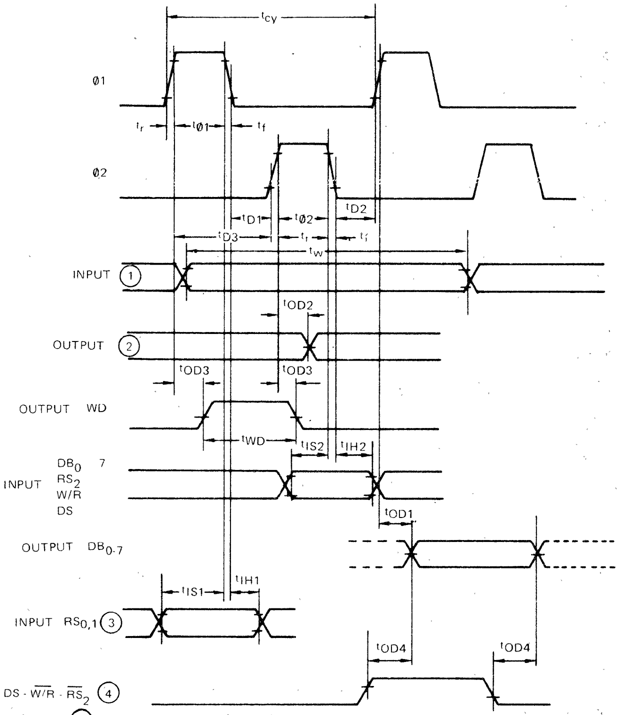
AC CHARACTERISTICS

$T_a = 0 - 70^\circ C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Clock Period	t_{CY}	480		2000	ns	
Clock Rise and Fall Times	t_r, t_f	0		50	ns	
ϕ_1 Pulse Width	$t_{\phi 1}$	60			ns	
ϕ_2 Pulse Width	$t_{\phi 2}$	90			ns	
ϕ_1 to ϕ_2 Delay	t_{D1}	0			ns	
ϕ_2 to ϕ_1 Delay	t_{D2}	70			ns	
Delay ϕ_1 to ϕ_2 Leading Edges	t_{D3}	100			ns	
Data Out Delay from ϕ_1	T_{OD1}			90	ns	1 TTL and $C_i = 30$ pF
Data Out Delay from ϕ_2 ①	t_{OD2}			200	ns	1 TTL and $C_i = 30$ pF
Data Out Delay from ϕ_2 ②				200	ns	2 TTL and $C_i = 50$ pF
WD Delay Time	t_{OD3}			120	ns	2 TTL and $C_i = 50$ pF
Data Out Delay from DS · $\overline{W/R}$ · $\overline{RS_2}$	t_{OD4}			200	ns	
Data Setup Time to ϕ_1	t_{IS_1}	150			ns	
Data Setup Time to ϕ_2	t_{IS_2}	120			ns	
Data Hold Time from ϕ_1	t_{IH_1}	10			ns	
Data Hold Time from ϕ_2	t_{IH_2}	10			ns	
WD pulse width	t_{WD}	t_{D3}-40	t_{D3}		ns	
Input pulse width ③	t_W	t_{CY}+150			ns	

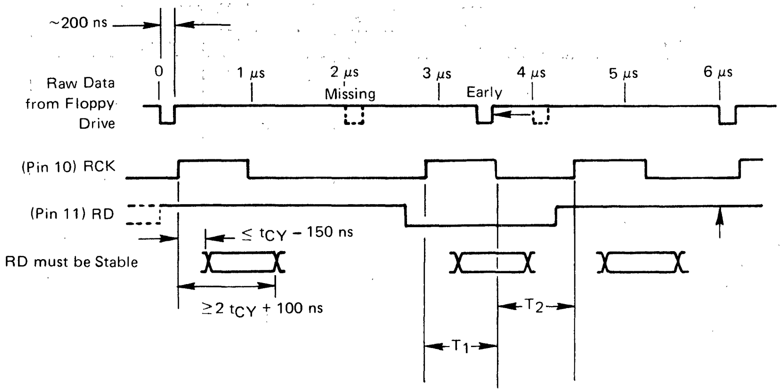
Notes: ① CKS, AWL, REQ, UA_0, UA_1, UB_0, UB_1.
② HLD, LCT, WFR, WE, SOS, SID.
③ IDX, RYA, RYB, RST, WFT, T_{00}, WCK, RCK.

TIMING WAVEFORMS



Notes: ① IDX, RYA, RYB, RST, WFT, TOO, WCK, RCK.
② CKS, WFR, SOS, SID, REQ, HLD, $UA_{0,1}$, $UB_{0,1}$, WE, LCT.
③ RS_0, RS_1 input must not make level transition within t_{IS1} and t_{IH1} times, or register contents may be modified.
④ The logic condition which places μPD372 information on DB_{0-7} is DS · $\overline{W/R}$ · $\overline{RS_2}$. Care must be taken to insure that this condition is not met inadvertently if DS, W/R and RS_2 are allowed to change state asynchronously.

READ CLOCK (RCK) AND READ DATA (RD) REQUIRED BY μPD372

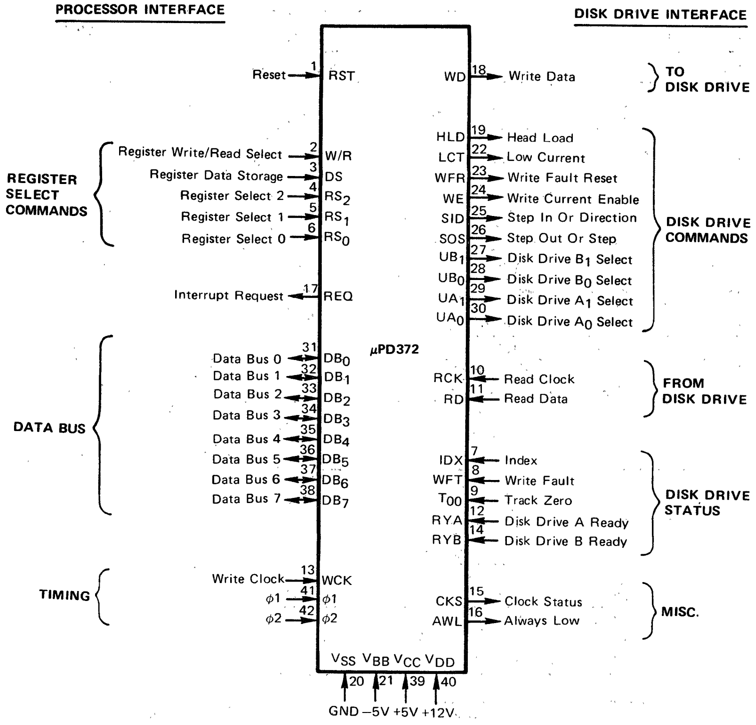


Notes: ① $t_{CY} = \phi 1$ Clock Period
② $T_1 \geq t_{CY} + 160$ ns
③ $T_2 \geq t_{CY} + 160$ ns

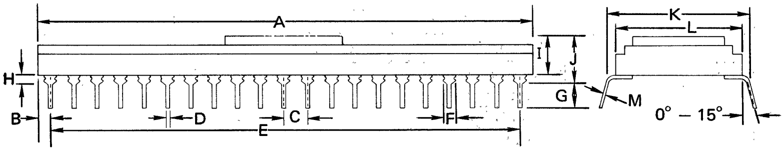
PIN IDENTIFICATION

PIN			INPUT/ OUTPUT	CONNECTION	FUNCTION
NO.	SYMBOL	NAME			
1	RST	Reset	Input	Processor	Initializes internal registers, counters and F/F's
2	W/R	Register Write/ Read Select			W/R = 1 implies $DB_{0\text{-}7}$ data written into μPD372 registers
3	DS	Data Strobe			$DB_{0\text{-}7}$ Write and read strobe
4-6	RS_ϕ RS_1 RS_2	Register Select			Internal Register Select
7	IDX	Index		FDD	Pulse Signal that indicates start of Disk track
8	WFT	Write Fault			Write Fault Signal
9	T_{00}	Track 00			Indicates that Head is positioned on Track 00
10	RCK	Read Clock			
11	RD	Read Data			
12	RYA	Ready A			Indicates that FDD A is Ready
13	WCK	Write Clock		Processor	
14	RYB	Ready B		FDD	Indicates that FDD B is Ready
15	CKS	Clock States	Output		
16	AWL	Always Low			Always a logic zero
17	REQ	Request		Processor	Interrupt Request
18	WD	Write Data		FDD	Serial Write Data (Clock & Data Bits)
19	HLD	Head Load			Command which causes R/W head to contact disk
22	LCT	Low Current			Command to lower write current for inner tracks
23	WFR	Write Fault Reset			Signal to reset write fault latch
24	WE	Write Enable			
25	SID	Step In or Direction			R/W head step control
26	SOS	Step Out or Step			R/W head step control
27-30	UA_0, UA_1 UB_0, UB_1	FDD Select			FDD Unit Select
31-38	$DB_{0\text{-}7}$	Data Bus	Input/ Output	Processor	Bi-directional data bus

PIN IDENTIFICATION (CONT.)



PACKAGE OUTLINE μPD372D



ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

BIT	SYMBOL	NAME	FUNCTION
WRITE REGISTER 0			
0		Not Used	
1	WFR	Write Fault Reset	Resets Pin 23 to Zero
2	LCT	Low Current	Sets Pin 22, Should be Zero for TRKS > 43
3	HLD	Head Load	Sets Pin 19, Loading FDD Head
4		Not Used	
5		Not Used	
6	MBL	Must Be Low	
7	RST	Reset	Software Reset, Same Effect as Pin 1
WRITE REGISTER 1			
0	UA_0	Unit A_0 Select	Device Select Pin 30
1	UA_1	Unit A_1 Select	Device Select Pin 29
2	UAS	Unit A Strobe	Strobe for Enabling UA_0 and OA_1 to be Loaded
3	CB_3	Clock Bit 3	Enables Clock Pulse #3 to be Written
4	CB_4	Clock Bit 4	Enables Clock Pulse #4 to be Written
5	CB_5	Clock Bit 5	Enables Clock Pulse #5 to be Written
6		Not Used	
7	CBS	Clock Bit Strobe	Enables Clock Bits to be Loaded
WRITE REGISTER 2			
0	WD_0	Write Data Bit 0	
1	WD_1	Write Data Bit 1	
2	WD_2	Write Data Bit 2	
3	WD_3	Write Data Bit 3	
4	WD_4	Write Data Bit 4	
5	WD_5	Write Data Bit 5	
6	WD_6	Write Data Bit 6	
7	WD_7	Write Data Bit 7	
WRITE REGISTER 3			
0	CCW	Cyclic Check Words	One During R/W, Zero for CRC Reset
1	CCG	Cyclic Check Generator Start	Starts CRC Generator in Write Mode
2	WER	Write Enable Reset	Resets Pin 24 to Zero
3	IXS	Index Start	Enable Index Hole Detection
4	WES	Write Enable Set	Sets Pin 24 to One
5	STT	Start	Enables Read and Write Operations to Occur
6	WCS	Write Clock Set	Write Clock Selected
7	RCS	Read Clock Set	Read Clock Selected
WRITE REGISTER 4			
0	UB_0	Unit B_0 Select	Device Select Pin 28
1	UB_1	Unit B_1 Select	Device Select Pin 27
2	UBS	Unit B Strobe	Strobe for Enabling UB_0, UB_1 to be Loaded
3		Not Used	
4		Not Used	
5	SOS	Step Out or Step	Sets Pin 26 to One
6	SID	Step In or Direction	Sets Pin 25 to One
7	STS	Step Strobe	Enables SOS and SID to be Loaded
WRITE REGISTER 5			
0–7		This Register Not Used	
		WRITE REGISTER 6	
0	DRR	Data Register Reset	Resets DRQ (RR_0 Bit 0)
1	IRR	Index Request Reset	Resets IRQ (RR_0 Bit 1)
2	TRR	Timer Request Reset	Resets TRQ (RR_0 Bit 2)
3		Not Used	
4		Not Used	
5		Not Used	
6		Not Used	
7		Not Used	

INTERNAL REGISTER IDENTIFICATION (CONT.)

BIT	SYMBOL	NAME	FUNCTION
READ REGISTER 0			
0	DRQ	Data Request	Read Data Byte from RR$_2$ or Write Data Byte into WR$_2$
1	IRQ	Index Request	Set by Physical Index Pulse
2	TRQ	Timer Request	Set by Every 512th Write CLK Pulse
3	ERR	Error	Logical OR of WFT + RYA + COR
4	UB$_0$	Drive B$_0$ Selected	
5	UB$_1$	Drive B$_1$ Selected	
6	RYB	Drive B Ready	Ready Signal from Pin 14
7	ALH	Always High	Always Contains a Logical One
READ REGISTER 1			
0	UA$_0$	Drive A$_0$ Selected	
1	UA$_1$	Drive A$_1$ Selected	
2	WFT	Write Fault	Indicates Status of Pin 8
3	RYA	Drive A Ready	Indicates Status of Pin 12
4	COR	Command Overrun	Processor Did Not Respond in Time to a DRQ
5	DER	Data Error	CRC Error During Read
6	T$_{00}$	Track Zero	Indicates Status of Pin 9
7	WRT	Write Mode	Indicates which Clock WCK or RCK has been Selected
READ REGISTER 2			
0	RD$_0$	Read Data Bit 0	
1	RD$_1$	Read Data Bit 1	
2	RD$_2$	Read Data Bit 2	
3	RD$_3$	Read Data Bit 3	
4	RD$_4$	Read Data Bit 4	
5	RD$_5$	Read Data Bit 5	
6	RD$_6$	Read Data Bit 6	
7	RD$_7$	Read Data Bit 7	

ADDRESSABLE INTERNAL REGISTERS

Data is transferred to the μPD372's internal addressable registers by signals W/R (Write=1, Read=0), DS (Data Strobe) and RS$_0$–RS$_2$ (Register Select 0, 1 and 2). Timing constraints for these signals are shown in the Timing Diagram. Diagram below shows register allocations and functional content.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS$_2$	RS$_1$	RS$_0$		7	6	5	4	3	2	1	0
					WRITE REGISTERS							
1	0	0	0	WR$_0$	RST	MBL	X	X	HLD	LCT	WFR	X
1	0	0	1	WR$_1$	CBS	X	CB$_5$	CB$_4$	CB$_3$	UAS	UA$_1$	UA$_0$
1	0	1	0	WR$_2$	WD$_7$	WD$_6$	WD$_5$	WD$_4$	WD$_3$	WD$_2$	WD$_1$	WD$_0$
1	0	1	1	WR$_3$	RCS	WCS	STT	WES	TXS	WER	CCG	CCW
1	1	0	0	WR$_4$	STS	SID	SOS	X	X	UBS	UB$_1$	UB$_0$
1	1	1	0	WR$_6$	X	X	X	X	X	TRR	IRR	DRR
					READ REGISTERS							
0	0	0	0	RR$_0$	ALH	RYB	UB$_1$	UB$_0$	ERR	TRQ	IRQ	DRQ
0	0	0	1	RR$_1$	WRT	T$_{00}$	DER	COR	RYA	WFT	UA$_1$	UA$_0$
0	0	1	0	RR$_2$	RD$_7$	RD$_6$	RD$_5$	RD$_4$	RD$_3$	RD$_2$	RD$_1$	RD$_0$

X = NOT USED

NEC Microcomputers, Inc.

NEC
μPD379

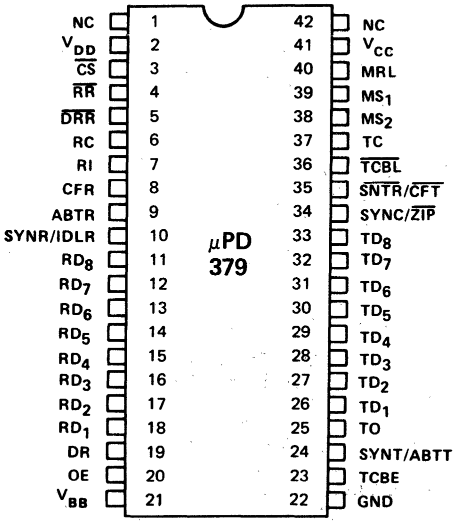
SYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION The μPD379 Synchronous Receiver/Transmitter is an MOS LSI monolithic circuit that performs all the receiving and transmitting functions associated with Basic and High Level Data Link Control Procedures. This circuit is fabricated using N-channel AL-Gate MOS technology, allowing all inputs and outputs to be directly TTL compatible. The operation mode, baud rate and synchronous character are changeable through the use of external control. The μPD379 is packaged in a 42 pin Dual-in-line ceramic package.

FEATURES

- Suitable for Synchronous Basic and High Level Data Link Control Procedures (BiSync or SDLC)
- Full or Half Duplex Operation
- Fully Double Buffered Transmit and Receive
- Directly TTL Compatible
- Three-State Data Outputs
- Programmable Sync Word
- Detection/Rejection of Flag, Abort and Idle Patterns
- Zero Insertion and Rejection
- Indication of Overrun and Underrun Errors
- 800K Bits/Sec Operating Speed

PIN CONFIGURATION



NC: NO CONNECTION

Rev/1

Basic Sync Mode Transmission

The Sync character may be 16 in hexadecimal or it may be set to any other pattern in the Closed Mode. When the mode control register is loaded with MS_1 = high and MS_2 = low, the μPD379 enters the Basic Sync mode from the Closed Mode. The Sync character is continuously transmitted until a transmission data character is loaded. After a data character is loaded, it is serialized and transmitted out from the TO (Transmitter Output) line. If an underrun occurs, Sync character(s) are again transmitted automatically until the next data character is loaded. Transmission data is sent out from LSB (TD_1) first to MSB (TD_8) last on the TO line.

Basic Sync Mode Receive

The RI (Receiver Input) line first searches for Sync characters. Once an 8-bit Sync character has been detected, the following received bits are treated as data characters and outputted on lines $RD_1 - RD_8$ in parallel.

When device operation is started, the receiver section should be first brought into Closed mode or should be reset in order to ensure synchronization.

SDLC Mode Transmission

Until a data character is loaded, the Flag pattern (7E in hexadecimal) is automatically transmitted continuously. After a data character is loaded, it is serialized and transmitted out from LSB (TD_1) to MSB (TD_8) on the TO line. In transmitting data characters, a dummy bit 0 is automatically inserted immediately following five (5) successive 1's. This is called Zero-Insertion and is performed in order to maintain synchronization with the receiver and to avoid duplication of Flag pattern in data characters. (Zero-Insertion may be prohibited optionally with the $\overline{\text{ZIP}}$ command, if necessary.) If an underrun occurs while data characters are being transmitted, an Abort pattern (FF in hexadecimal) and then a Flag pattern are automatically transmitted. After that, the Flag pattern is again automatically transmitted until the next data character is loaded.

If a low level is placed on the $\overline{\text{CFT}}$ (Closing Flag Transmit) line while a data character is being transmitted, a Closing Flag will be transmitted immediately following transmission of the current data character.

SDLC Mode Receive

First, the Flag pattern is searched for on the RI line. Once a Flag pattern is detected, inserted zero's are rejected from all the following characters except Flag, Abort (7 to 14 successive 1's) and Idle (15 successive 1's) patterns, and then deserialized and output on the $RD_1 - RD_8$ lines in parallel.

If an overrun occurs, all the following data inputs are neglected and the μPD379 goes back to the first stage to search for the next Flag pattern.

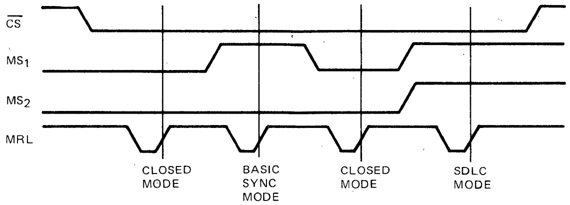
Closed Mode

When there is a change of mode, it must pass through the closed mode. In the closed mode, the following input signals may be used:

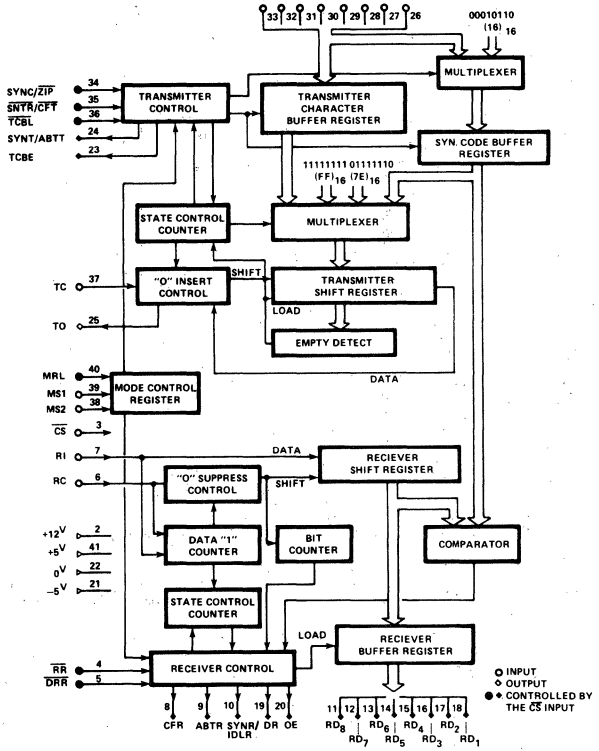
$\overline{\text{CS}}$, SYNC, $\overline{\text{TCBL}}$, MS1, MS2, MRL, $TD_1 - TD_8$

After leaving the closed mode, Sync characters are transmitted synchronously with the rising edge of TC. The receiver operates synchronously with the falling edge of RC, after $\overline{\text{RR}}$ = 1.

The following timing diagram shows how mode changes may be accomplished.



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	0V to +8.0V ①
All Input Voltages	0V to +8.0V ①
Supply Voltage V_{CC}	0V to +8.0V ①
Supply Voltage V_{DD}	0V to +16.0V ①
Supply Voltage V_{BB}	-10.0V to 0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

Note: ① $V_{BB} = -5 \pm 5\%$

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Frequency	f_C	DC		800	KHz	TC, RC
Pulse Width	t_{PW}					TC, RC
		250			ns	MRL
		250			ns	TCBL
		250			ns	SNTR/CFT
		250			ns	ZIP
		400			ns	RR
		250			ns	DRR
Setup Time	$t_{SET\ UP}$	250			ns	
Hold Time	t_{HOLD}	150			ns	
Rise Time	t_r			150	ns	
Fall Time	t_f			150	ns	
Pulse Interval	t_{cc}	100			ns	
Output Delay Time	t_{pd1}		180	270	ns	$C_L = 20$ pf
	t_{pd2}		410	600	ns	1 TTL Load
Fan Out	N			1		Standard TTL Load

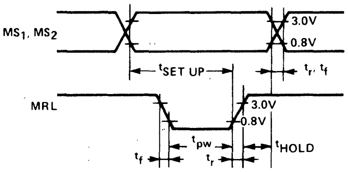
*50% Duty Cycle

PIN IDENTIFICATION

PIN		FUNCTION	
NO.	SYMBOL	BASIC SYNC MODE	SDLC MODE
1	NC	No Connection	
2	V_{DD}	+12V Power Supply	
3	$\overline{\text{CS}}$	Chip Select – When "1", the following inputs are disabled and the outputs are put into the high impedance state: (Input Disabled) $\overline{\text{RR}}$, $\overline{\text{DRR}}$, SYNC/$\overline{\text{ZIP}}$, $\overline{\text{SNTR}}$/$\overline{\text{CFT}}$, $\overline{\text{TCBL}}$, MRL; (Output-High Impedance) CFR, ABTR, SYNR/IDLR, RD_1 – RD_8, DR, OE, TCBE, CYNT/ABTT	
4	$\overline{\text{RR}}$	Receiver Reset – Receiver portion is reset with a "0" and operation is stopped RD_1 – RD_8 – – – – "1" CFR, ABTR, SYNR/IDLR, AR, OE – – – – "0"	
5	$\overline{\text{DRR}}$	Data Received Reset – Resets DR flag to "0"	
6	RC	Receiver Clock – Receiver clock input. Trailing edge of clock is located in the center of receiver input bits (RI).	
7	RI	Receiver Input – Received data serial input	
8	CFR	(Normally "0")	Closing Flag Received – Goes high whenever a Flag has been received during data reception. Goes low on the rising edge of DR or OE commands
9	ABTR	("0" Constant)	Abort Received – Becomes "1" when 7 – 14 continuous "1"s are received, after receiving the flag. Goes low on the rising edge of DR or OE commands.
10	SYNR IDLR	Sync Character Received – Goes high when synchronization has occurred, or whenever the contents of the Sync Character Buffer and the contents of the Receiver Character Buffer coincide. Goes low when DR goes high and the RD_1 – RD_8 outputs are different from the Sync Character.	Idle Pattern Received – Becomes "1" (Idle) when it receives 15 consecutive "1"s. Goes low on the rising edge of DR or OE outputs.
11 – 18	RD_8 – RD_1	Receiver Data Outputs – Received character output terminal (RD_1:LSB RD_8:MSB)	
19	DR	Data Received – Goes high when the received character has been transferred from the Receiver Shift Register to the Receiver Buffer Register	
		DR does not go high for the first Sync Character input. It is reset when DRR is driven low.	DR does not go high for Flag, Abort or Idle Patterns. It is reset when (1) $\overline{\text{DRR}}$ = "0", (2) On the rising edge of OE, (3) Seven (7) successive "1"s have been received.
20	OE	Overrun Error – OE = "1" shows that DR was still high when the received character is moved from the receiving shift register to the receiving buffer register	
		OE is reset if DR is low when the received character is transferred from the Receiver Shift Register to the Receiver Buffer Register	It is reset on the rising edge of DR
21	V_{BB}	–5V Power Supply	
22	V_{SS}	Ground	
23	TCBE	Transmitter Character Buffer Register Empty – TCBE = "1" when the transmitter character buffer is empty.	
		TCBE is reset when $\overline{\text{TCBL}}$ is driven low	It is reset when: (1) $\overline{\text{TCBL}}$ = "0", (2) When $\overline{\text{CFT}}$ = "0" in the data transmission mode, (3) One-half bit before ABTT goes high.
24	SYNT ABTT	SYNC Character Transmit – SYNT = "1" when a synchronous character is being transmitted. It is reset when: (1) $\overline{\text{SNTR}}$ = "0", (2) when transmission of data commences	Abort Pattern Transmit – ABTT = "1" when an Abort Pattern is being transmitted
25	TO	Transmitter Output – Transmitter data output. TO = "1" in the closed mode.	
26 – 33	TD_1 – TD_8	Transmitter Data Inputs – Transmitter character input. (TD_1 = LSB, TD_8 = MSB)	
34	SYNC $\overline{\text{ZIP}}$	SYNC Character – In the Closed Mode, the SYNC line is used to select a SYNC character to be loaded into the SYNC Character Buffer. The selected SYNC character is loaded into the buffer on the rising edge of TCBL and is selected as follows: (1) When SYNC = "0", the character placed on the TD_1 – TD_8 inputs is loaded, (2) When SYNC = "1", 16 Hexadecimal is loaded.	Zero Insertion Prohibit – When $\overline{\text{ZIP}}$ is driven low, zero-insertion will be prohibited for all subsequent data characters until a Closing Flag or an Abort Pattern is transmitted.
35	$\overline{\text{SNTR}}$ $\overline{\text{CFT}}$	SYNC Character Transmit Reset – When $\overline{\text{SNTR}}$ is driven low, SYNT is reset to "0".	Closing Flag Transmit – During transmission, $\overline{\text{CFT}}$ low causes the following operations to occur: (1) TCBE Output is reset to "0", (2) The Closing Flag will be transmitted after the end of transmission of the current data character.
36	$\overline{\text{TCBL}}$	Transmitter Character Buffer Load – (1) In the closed Mode: the SYNC Character Buffer is loaded on the rising edge of $\overline{\text{TCBL}}$. If the SYNC input is low, the buffer is loaded with the data on the TD_1 – TD_8 inputs; if SYNC is high, the buffer is loaded with (16) Hex. (2) In the Basic SYNC or SDLC Modes: When $\overline{\text{TCBL}}$ is driven low (a) TCBE is reset to "0" and (b) the data character on the TD_1 – TD_8 inputs is loaded into the Transmitter Character Buffer. The loaded character is latched on the rising edge of $\overline{\text{TCBL}}$.	
37	TC	Transmitter Clock – Clock input for transmission.	
38	MS_2	Mode Select 2	
39	MS_1	Mode Select 1 Used to select one of three modes. MS_1 MS_2 MODE L L Closed Mode L H Closed Mode H L Basic Synchronous Mode H H SDLC Synchronous Mode In the closed mode TO and RD_1 – RD_8 are high, all other outputs are low.	
40	MRL	Mode Control Register Load – When MRL is low, the operational mode is selected by the current status of MS_1 and MS_2. When MRL goes high, the operational mode is latched based upon the status of MS_1 and MS_2.	
41	V_{CC}	+5V Power Supply	
42	NC	No Connection	

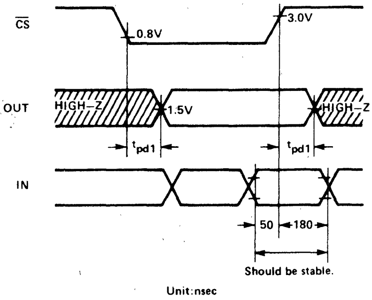
TIMING WAVEFORMS

MODE SELECT

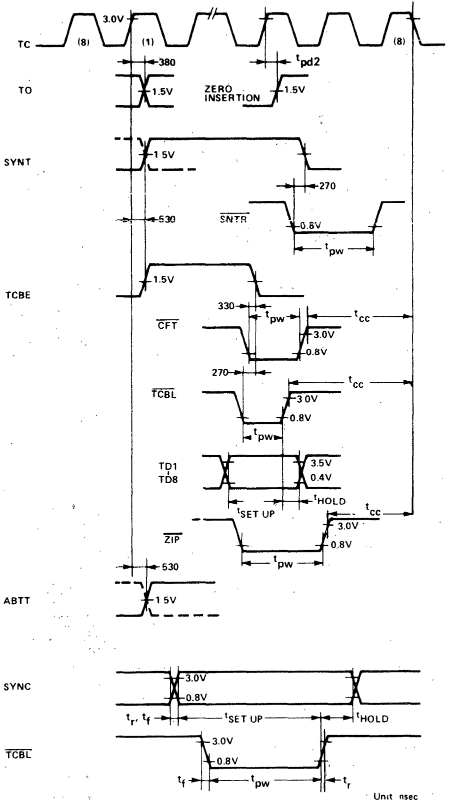


MODE	MS_1	MS_2	MRL
Closed	0	0 or 1	⊔
Basic Sync	1	1	⊔
SDLC	1	1	⊔

CHIP SELECT

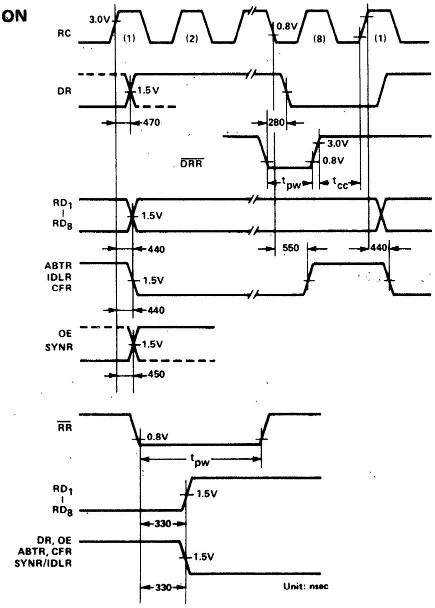


TRANSMITTER SECTION



TIMING WAVEFORMS (CONT.)

RECEIVER SECTION



DC CHARACTERISTICS

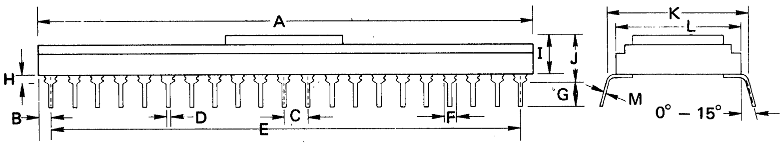
T_a = 0°C to +70°C, V_{DD} = 12V + 5%, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input High Voltage	V_{IH}	3.0		V_{DD}	V	With Built-in pull-up resistors
Input Low Voltage	V_{IL}			0.8	V	
Output Leakage Current	I_{OL}	–20		20	μA	-V_O = 0.4 to 3.5V (CS)= 3.5V
Output High Voltage	V_{OH}	3.5			V	I_{OH} = –100μA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
Input Low Current	I_{IL}			–1.4	mA	V_{IL} = 0.4V
V_{DD} Supply Current	I_{DD}		15	20	mA	
V_{CC} Supply Current	I_{CC}		40	65	mA	
V_{BB} Supply Current	I_{BB}		–0.2	–2.0	mA	
Fan-out	N			1		Standard TTL Load

CAPACITANCE

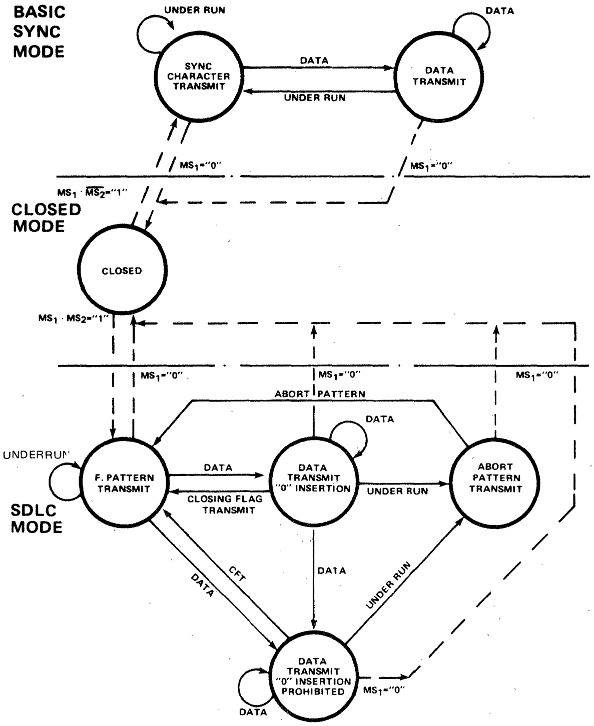
Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input Capacitance	C_{IN}			20	pf	f = 1 MHz
Output Capacitance	C_{OUT}			20	pf	f = 1 MHz

PACKAGE OUTLINE μPD379D

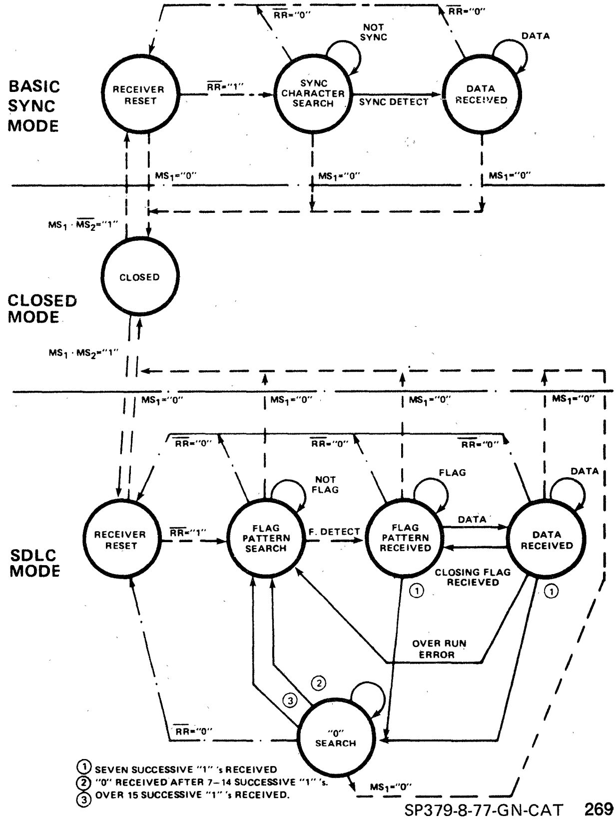


ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

TRANSMITTER STATE DIAGRAM



RECEIVER STATE DIAGRAM



① SEVEN SUCCESSIVE "1" 's RECEIVED
② "0" RECEIVED AFTER 7–14 SUCCESSIVE "1" 's.
③ OVER 15 SUCCESSIVE "1" 's RECEIVED.

7

NEC

NEC Microcomputers, Inc.

μPD765

SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The μPD765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the μPD765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μPD8257. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the μPD765 and DMA controller.

There are 15 separate commands which the μPD765 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

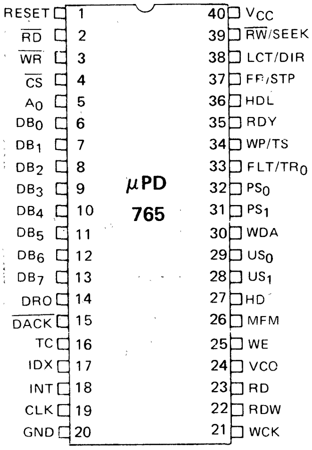
Read Data
Read ID
Read Deleted Data
Read a Track
Scan Equal
Scan High or Equal
Scan Low or Equal
Specify
Write Data
Format a Track
Write Deleted Data
Seek
Recalibrate (Restore to Track 0)
Sense Interrupt Status
Sense Drive Status

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The μPD765 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

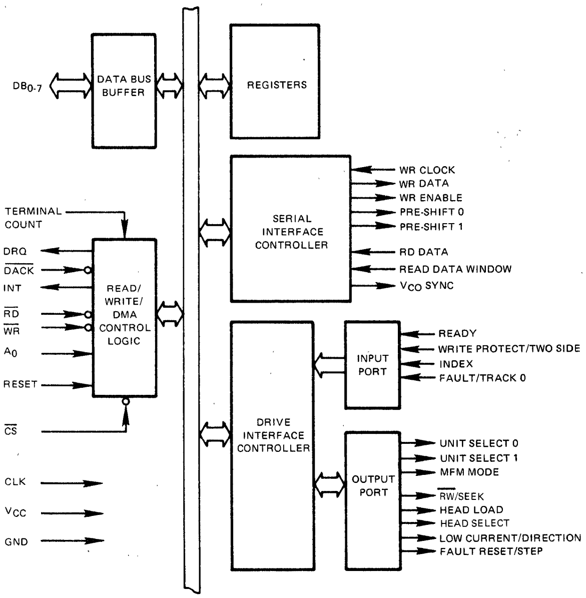
- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability — Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most Microprocessors Including 8080A, 8085A, μPD780 (Z80™)
- Single Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40 Pin Plastic Dual-in-Line Package

PIN CONFIGURATION



TM:Z80 is a registered trademark of Zilog, Inc.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts
Power Dissipation	1 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP①	MAX		
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.5		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -150 μA for Data Bus I_{OH} = -80 μA for other outputs
Input Low Voltage (CLK + WR Clock)	$V_{IL(\Phi)}$	-0.5		0.8	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\Phi)}$	V_{CC} - 0.75		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}		85	130	mA	
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = V_{CC}
				-10	μA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			-10	μA	V_{OUT} = 0V

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

PIN IDENTIFICATION

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO.	SYMBOL	NAME			
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low).
2	$\overline{RD}$	Read	Input①	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input①	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input①	Processor	Selects Data Reg (A_0=1) or Status Reg (A_0=0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input/① Output	Processor	Bi-Directional 8-bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRQ="1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high).
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1".
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1", FM mode when "0".
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high), Head 0 selected when "0" (low).
28,29	US_1, US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31,32	PS_1, PS_0	Precompensation (pre-shift)	Output	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode, and Two Side Media in Seek mode.
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Flt Reset/Step	Output	FDD	Resets fault F.F. in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			D.C. Power

Note: ① Disabled when CS = 1.

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP 1	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	Φ_{CY}	1.0	8.0	9.0	MHz	
Clock Active (High)	Φ_0	35			ns	
Clock Rise Time	Φ_r			20	ns	
Clock Fall Time	Φ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓	T_{AR}	30			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑	T_{RA}	5.0			ns	
$\overline{RD}$ Width	T_{RR}	300			ns	
Data Access Time from $\overline{RD}$ ↓	T_{RD}			200	ns	
DB to Float Delay Time from $\overline{RD}$ ↑	T_{DF}	20		100	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓	T_{AW}	50			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑	T_{WA}	30			ns	
$\overline{WR}$ Width	T_{WW}	300			ns	
Data Set Up Time to $\overline{WR}$ ↑	T_{DW}	250			ns	
Data Hold Time from $\overline{WR}$ ↑	T_{WD}	30			ns	
INT Delay Time from $\overline{RD}$ ↑	T_{RI}			500	ns	
INT Delay Time from $\overline{WR}$ ↑	T_{WI}			500	ns	
DRQ Cycle Time	T_{MCY}	13			μs	
DRQ Delay Time from $\overline{DACK}$ ↑	T_{AM}			1.0	μs	
$\overline{WR}$ or $\overline{RD}$ Response Time from DRQ ↑	T_{RWM}	1.0			μs	
TC Width	T_{TC}	300			ns	
Rest Width	T_{RST}	3.0			μs	
WCK Cycle Time	T_{CY}		2 or 4 ② 1 or 2		μs	MFM = 0 MFM = 1
WCK Active Time (High)	T_0	150	250	350	ns	
WCK Rise Time	T_r			30	ns	
WCK Fall Time	T_f			30	ns	
Pre-Shift Delay Time from WCK ↑	T_{CP}	20		150	ns	
WDA Delay Time from WCK ↑	T_{CD}	20		150	ns	
RDD Active Time (High)	T_{RDD}	100			ns	
Window Cycle Time	T_{WCY}		2.0 1.0		μs	MFM = 0 MFM = 1
Window Hold Time to/from RDD	T_{RDW} T_{WRD}	100			ns	
$US_{0,1}$ Hold Time to RW/SEEK ↑	T_{US}	12			μs	
SEEK/RW Hold Time to LOW CURRENT/DIRECTION ↑	T_{SD}	7			μs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑	T_{DST}	1.0			μs	8 MHz Clock Period
$US_{0,1}$ Hold Time from FAULT RESET/STEP ↑	T_{STU}	1.0			μs	
STEP Active Time (High)	T_{STP}		5.0		μs	
LOW CURRENT/DIRECTION Hold Time from FAULT RESET/STEP ↓	T_{STD}	5.0			μs	
STEP Cycle Time	T_{SC}	③		③	ms	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	μs	8 MHz Clock Period

Notes: ① Typical values for $T_a = 25°C$ and nominal supply voltage.

② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.

③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.

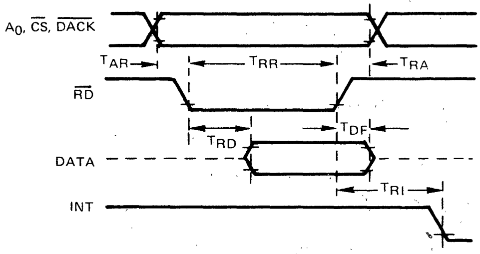
CAPACITANCE

$T_a = 25°C$; f = 1 MHz

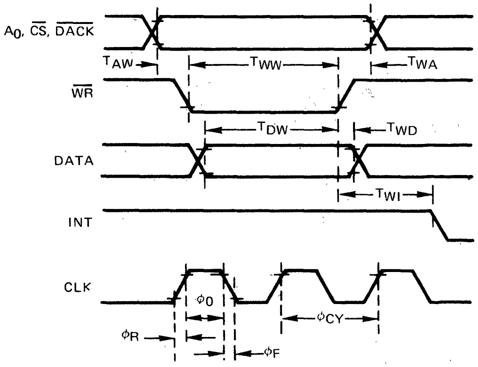
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Capacitance	$C_{IN(\Phi)}$			35	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING WAVEFORMS

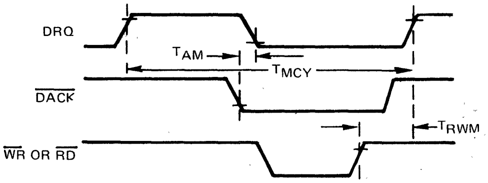
PROCESSOR READ OPERATION



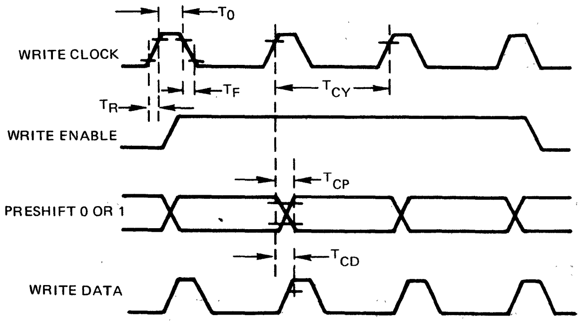
PROCESSOR WRITE OPERATION



DMA OPERATION



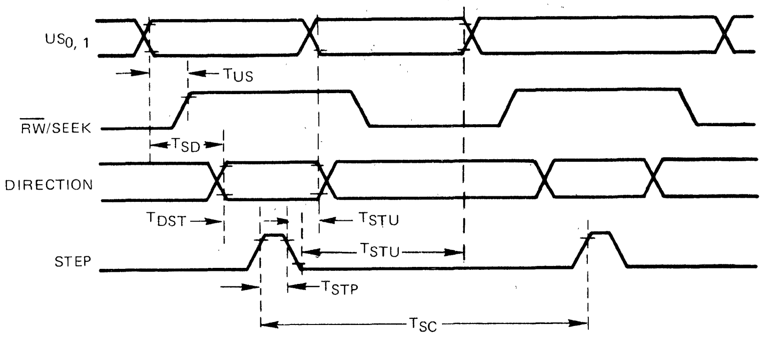
FDD READ OPERATION



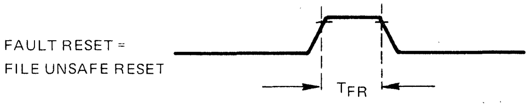
	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

TIMING WAVEFORMS (CONT.)

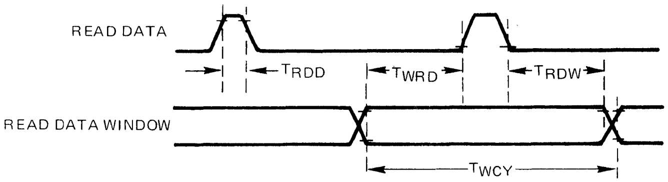
SEEK OPERATION



FLT RESET

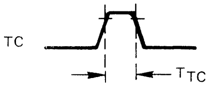


FDD READ OPERATION

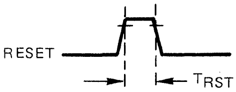


Note: Either polarity data window is valid.

TERMINAL COUNT



RESET



INTERNAL REGISTERS

The µPD765 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and µPD765.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

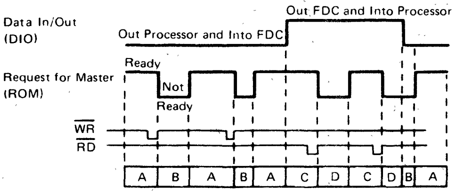
A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

INTERNAL REGISTERS (CONT.)

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB$_0$	FDD 0 Busy	D$_0$B	FDD number 0 is in the Seek mode.
DB$_1$	FDD 1 Busy	D$_1$B	FDD number 1 is in the Seek mode.
DB$_2$	FDD 2 Busy	D$_2$B	FDD number 2 is in the Seek mode.
DB$_3$	FDD 3 Busy	D$_3$B	FDD number 3 is in the Seek mode.
DB$_4$	FDC Busy	CB	A read or write command is in process.
DB$_5$	Non-DMA mode	NDM	The FDC is in the non-DMA mode.
DB$_6$	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB$_7$	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus.



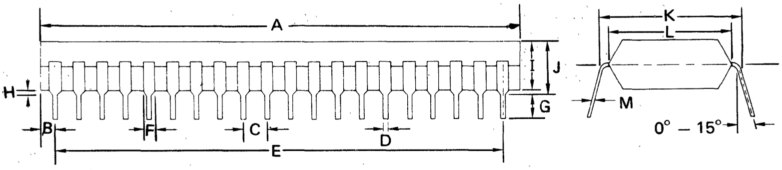
Notes. A – Data register ready to be written into by processor

B – Data register not ready to be written into by processor

C – Data register ready for next data byte to be read by the processor

D – Data register not ready for next data byte to be read by processor

PACKAGE OUTLINE μPD765C



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

COMMAND SEQUENCE

The μPD765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the μPD765 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

INSTRUCTION SET ① ②

PHASE	R/W	DATA BUS								REMARKS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS								REMARKS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information during Execution Phase
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire cylinder
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.
② A_0 should equal binary 1 for all operations.
③ X = Don't care, usually made to equal binary 0.

INSTRUCTION SET (CONT.)

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
SCAN HIGH OR EQUAL										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of seek-operation about the FDC
	R	PCN								
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	ST 3								Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	NCN								
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	Invalid Codes								Invalid Command Codes (NoOp — FDC goes into Standby State)
Result	R	ST 0								ST 0 = $80_{(16)}$

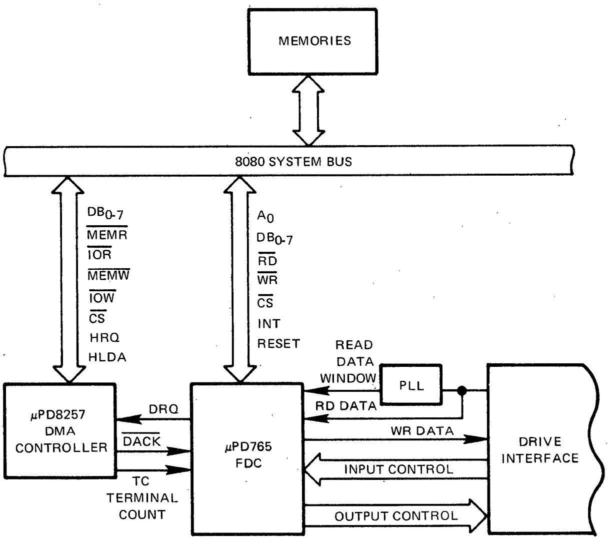
COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1)
C	Cylinder Number	C stands for the current selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync. Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 256 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (0 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)

COMMAND SYMBOL DESCRIPTION (CONT.)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Must be defined for each of the four drives.
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

SYSTEM CONFIGURATION



PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command. A command may be truncated (prematurely ended) by simply sending a Terminal Count signal to pin 16 (TC = 1). This is a convenient means of ensuring that the processor may always get the μPD765's attention even if the disk system hangs up in an abnormal manner.

FUNCTIONAL DESCRIPTION OF COMMANDS

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 0, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Status Register 2 to a 1 (high), and terminates the Read Data Command.

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the DM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 µs in the FM Mode, and every 13 µs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	C + 1	NC	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	NC	R = 01	NC
1	1A 0F 08	Sector 1 to 25 at Side 0 Sector 1 to 14 at Side 0 Sector 1 to 7 at Side 0	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 0 Sector 15 at Side 0 Sector 8 at Side 0	NC	LSB	R = 01	NC
	1A 0F 08	Sector 1 to 25 at Side 1 Sector 1 to 14 at Side 1 Sector 1 to 7 at Side 1	NC	NC	R + 1	NC
	1A 0F 08	Sector 26 at Side 1 Sector 15 at Side 1 Sector 8 at Side 1	C + 1	LSB	R = 01	NC

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.
2 LSB (Least Significant Bit): The least significant bit of H is complemented.

Table 2: ID Information When Processor Terminates Command

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified heat settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 31 µs in the FM mode, and every 15 µs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the MD flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire contents of the track are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data on the track, Gap bytes, Address Marks and Data are all read as a continuous data stream. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when EOT number of sectors have been read (EOT_{max} = FF_{hex} = 255_{dec}). If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mask) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively).

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole cylinder until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respecitvely.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	REMARKS
FM Mode	128 bytes/Sector	00	1A$_{(16)}$	07$_{(16)}$	1B$_{(16)}$	IBM Diskette 1
	256	01	0F$_{(16)}$	0E$_{(16)}$	2A$_{(16)}$	IBM Diskette 2
	512	02	08	1B$_{(16)}$	3A$_{(16)}$	
FM Mode	1024 bytes/Sector	03	04	–	–	
	2048	04	02	–	–	
	4096	05	01	–	–	
MFM Mode	256	01	1A$_{(16)}$	0E$_{(16)}$	36$_{(16)}$	IBM Diskette 2D
	512	02	0F$_{(16)}$	1B$_{(16)}$	54$_{(16)}$	
	1024	03	08	35$_{(16)}$	74$_{(16)}$	IBM Diskette 2D
	2048	04	04	–	–	
	4096	05	02	–	–	
	8192	06	01	–	–	

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leqslant D_{Processor}$, or $D_{FDD} \geqslant D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \nless D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \ngtr D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
    a. Read Data Command
    b. Read a Track Command
    c. Read ID Command
    d. Read Deleted Data Command
    e. Write Data Command
    f. Format a Cylinder Command
    g. Write Deleted Data Command
    h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 0 to 240 ms in increments of 16 ms (00 = 0 ms, 01 = 16 ms, 02 = 32 ms, etc.). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 256 ms in increments of 2 ms (00 = 2 ms, 01 = 4 ms, 02 = 6 ms, etc.).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. **A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.**

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

STATUS REGISTER IDENTIFICATION

BIT			DESCRIPTION
NO.	NAME	SYMBOL	
			STATUS REGISTER 0
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 0	US 0	
			STATUS REGISTER 1
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

STATUS REGISTER IDENTIFICATION (CONT.)

BIT			DESCRIPTION
NO.	NAME	SYMBOL	
STATUS REGISTER 1 (CONT.)			
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

NEC Microcomputers, Inc.

NEC
μPD8155
μPD8156

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

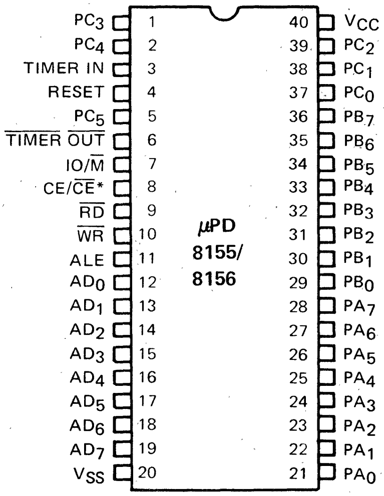
DESCRIPTION

The μPD8155 and μPD8156 are μPD8085A family components having 256 X 8 Static RAM, 3 programmable I/O ports and a programmable timer. They directly interface to the multiplexed μPD8085A bus with no external logic. The μPD8155 has an active low chip enable while the μPD8156 is active high.

FEATURES

- 256 X 8-Bit Static RAM
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Single Power Supplies: +5 Volt
- Directly Interfaces to the μPD8085A
- Available in 40 Pin Plastic Packages

PIN CONFIGURATION



*μPD8155: $\overline{\text{CE}}$
μPD8156: CE

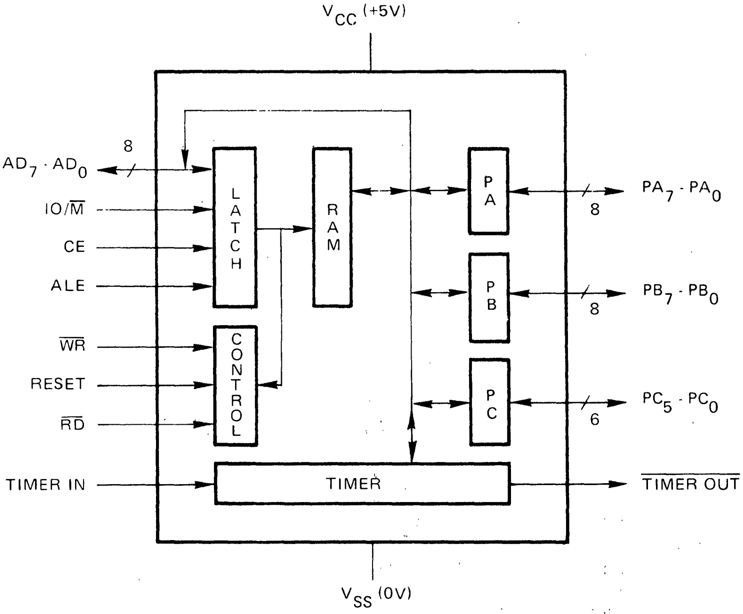
FUNCTIONAL DESCRIPTION

The μPD8155 and μPD8156 contain 2048 bits of Static RAM organized as 256 X 8. The 256 word memory location may be selected anywhere within the 64K memory space by using combinations of the upper 8 bits of address from the μPD8085A as a chip select.

The two general purpose 8-bit ports (PA and PB) may be programmed for input or output either in interrupt or status mode. The single 6-bit port (PC) may be used as control for PA and PB or general purpose input or output port. The μPD8155 and μPD8156 are programmed for their system personalities by writing into their Command/Status Registers (C/S) upon system initialization.

The timer is a single 14-bit down counter which is programmable for 4 modes of operation; see Timer Section.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Plastic Package)	−40°C to +125°C
Voltage on Any Pin	−0.3 to +7 Volts①
Power Dissipation	1.5 W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 5 39, 38, 37	PC_3, PC_4, PC_5 PC_2, PC_1, PC_0	Port C	Used as control for PA and PB or as a 6-bit general purpose port
3	TIMER IN	Timer Clock In	Clock input to the 14-bit binary down counter
4	RESET	Reset In	From μPD8085A system reset to set PA, PB, PC to the input mode
6	$\overline{\text{TIMER}}$ $\overline{\text{OUT}}$	Timer Counter Output	The output of the timer function
7	IO/$\overline{\text{M}}$	I/O or Memory Indicator	Selects whether operation to and from the chip is directed to the internal RAM or to I/O ports
8	CE/$\overline{\text{CE}}$	Chip Enable	Chip Enable Input. Active low for μPD8155 and active high for μPD8156
9	$\overline{\text{RD}}$	Read Strobe	Causes Data Read
10	$\overline{\text{WR}}$	Write Strobe	Causes Data Write
11	ALE	Address Low Enable	Latches low order address in when valid
12-19	$AD_0 - AD_7$	Low Address/Data	3-State address/data bus to interface directly to μPD8085A
20	V_{SS}	Ground	Ground Reference
21-28	$PA_0 - PA_7$	Port A	General Purpose I/O Port
29-36	$PB_0 - PB_7$	Port B	General Purpose I/O Port
40	V_{CC}	5 Volt Input	Power Supply

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$

PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP	MAX		
Input Low Voltage		V_{IL}	−0.5		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage		V_{OL}			0.45	V	$I_{OL} = 2$ mA
Output High Voltage		V_{OH}	2.4			V	$I_{OH} = 400$ μA
Input Leakage		I_{IL}			±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current		I_{LO}			±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
V_{CC} Supply Current		I_{CC}			180	mA	
Chip Enable Leakage	μPD8155	I_{IL} (CE)			+100	μA	$V_{IN} = V_{CC}$ to 0V
	μPD8156	I_{IL}(CE)			−100	μA	

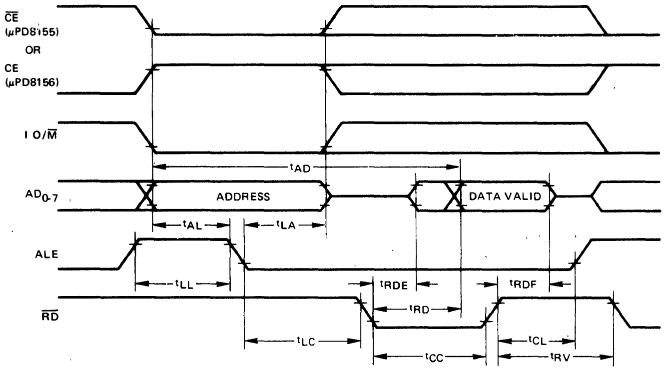
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

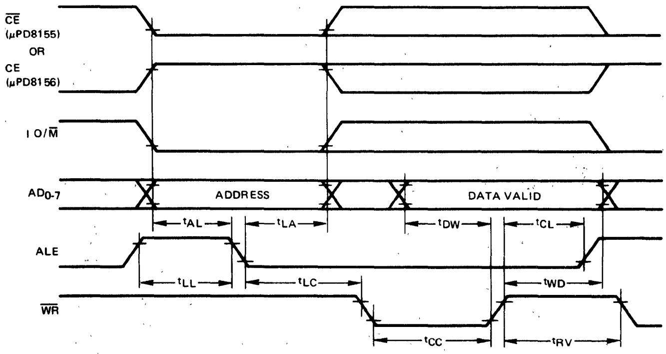
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Address to Latch Set Up Time	t_{AL}	50			ns	150 pF Load
Address Hold Time after Latch	t_{LA}	80			ns	
Latch to READ/WRITE Control	t_{LC}	100			ns	
Valid Data Out Delay from READ Control	t_{RD}			170	ns	
Address Stable to Data Out Valid	t_{AD}			400	ns	
Latch Enable Width	t_{LL}	100			ns	
Data Bus Float After READ	t_{RDF}	0		100	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20			ns	
READ/WRITE Control Width	t_{CC}	250			ns	
Data In to WRITE Set Up Time	t_{DW}	150			ns	
Data In Hold Time After WRITE	t_{WD}	0			ns	
Recovery Time Between Controls	t_{RV}	300			ns	
WRITE to Port Output	t_{WP}			400	ns	
Port Input Setup Time	t_{PR}	70			ns	
Port Input Hold Time	t_{RP}	50			ns	
Strobe to Buffer Full	t_{SBF}			400	ns	
Strobe Width	t_{SS}	200			ns	
READ to Buffer Empty	t_{RBE}			400	ns	
Strobe to INTR On	t_{SI}			400	ns	
READ to INTR Off	t_{RDI}			400	ns	
Port Setup Time to Strobe Strobe	t_{PSS}	50			ns	
Port Hold Time After Strobe	t_{PHS}	120			ns	
Strobe to Buffer Empty	t_{SBE}			400	ns	
WRITE to Buffer Full	t_{WBF}			400	ns	
WRITE to INTR Off	t_{WI}			400	ns	
TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low	t_{TL}			400	ns	
TIMER-IN to $\overline{\text{TIMER-OUT}}$ High	t_{TH}			400	ns	
Data Bus Enable from READ Control	t_{RDE}	10			ns	

TIMING WAVEFORMS

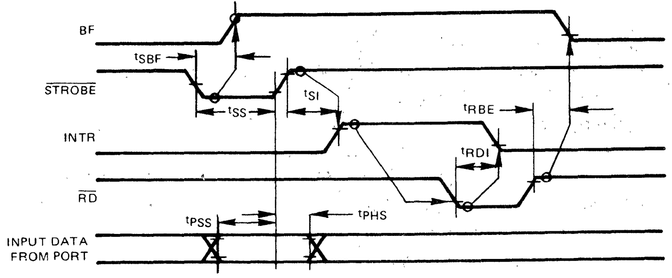
READ CYCLE

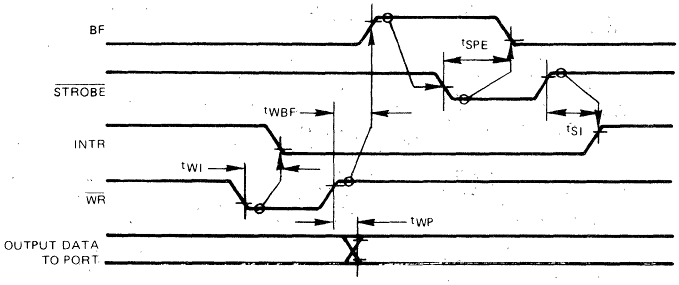


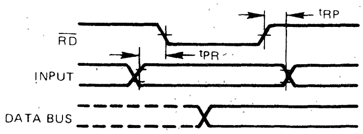
WRITE CYCLE

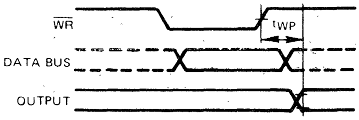


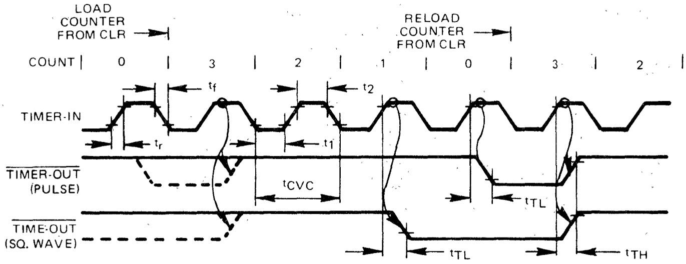
TIMING WAVEFORMS (CONT.)


STROBED INPUT MODE


STROBED OUTPUT MODE


BASIC INPUT MODE


BASIC OUTPUT MODE


TIMER OUTPUT

COUNTDOWN FROM 3 TO 0

t_{CYC}	320 ns MIN.
t_{RISE} & t_{FALL}	30 ns MAX.
t_1	80 ns MIN.
t_2	120 ns MIN.
t_{TL}	TIMER-IN TO $\overline{\text{TIMER-OUT}}$ LOW (TO BE DEFINED).
t_{TH}	TIMER-IN TO $\overline{\text{TIMER-OUT}}$ HIGH (TO BE DEFINED).

COMMAND STATUS REGISTER

The Command Status Register is an 8-bit register which must be programmed before the μPD8155/8156 may perform any useful functions. Its purpose is to define the mode of operation for the three ports and the timer. Programming of the device may be accomplished by writing to I/O address XXXXX000 (X denotes don't care) with a specific bit pattern. Reading of the Command Status Register can be accomplished by performing an I/O read operation at address XXXXX000. The pattern returned will be a 7-bit status report of PA, PB and the Timer. The bit patterns for the Command Status Register are defined as follows:

COMMAND STATUS WRITE

TM2	TM1	IEB	IEA	PC$_2$	PC$_1$	PB	PA

where:

TM2-TM1	Define Timer Mode
IEB	Enable Port B Interrupt
IEA	Enable Port A Interrupt
PC$_2$-PC$_1$	Define Port C Mode
PB/PA	Define Port B/A as In or Out ①

The Timer mode of operation is programmed as follows during command status write:

TM2	TM1	TIMER MODE
0	0	Don't Affect Timer Operation
0	1	Stop Timer Counting
1	0	Stop Counting after TC
1	1	Start Timer Operation

Interrupt enable status is programmed as follows:

IEB/IEA	INTERRUPT ENABLE PORT B/A
0	No
1	Yes

Port C may be placed in four possible modes of operation as outlined below. The modes are selected during command status write as follows:

PC$_2$	PC$_1$	PORT C MODE
0	0	ALT 1
0	1	ALT 3
1	0	ALT 4
1	1	ALT 2

The function of each pin of port C in the four possible modes is outlined as follows:

PIN	ALT 1	ALT 2	ALT 3 ②	ALT 4 ②
PC0	IN	OUT	A INTR	A INTR
PC1	IN	OUT	A BF	A BF
PC2	IN	OUT	A $\overline{STB}$	A $\overline{STB}$
PC3	IN	OUT	OUT	B INTR
PC4	IN	OUT	OUT	B BF
PC5	IN	OUT	OUT	B $\overline{STB}$

Notes: ① PB/PA Sets Port B/A Mode: 0 = Input; 1 = Output

② In ALT 3 and ALT 4 mode the control signals are initialized as follows:

CONTROL	INPUT	OUTPUT
$\overline{STB}$ (Input Strobe)	Input Control	Input Control
INTR (Interrupt Request)	Low	High
BF (Buffer Full)	Low	Low

COMMAND STATUS REGISTER (CONT.)

COMMAND STATUS READ

☒	TI	INTE B	B BF	INTR B	INTE A	A BF	INTR A

Where the function of each bit is as follows:

TI	Defines a Timer Interrupt. Latched high at TC and reset after reading the CS register or starting a new count.
INTE B/A	Defines If Port B/A Interrupt is Enabled. High = enabled.
B/A BF	Defines If Port B/A Buffer is Full-Input Mode or Empty-Output Mode. High = active.
INTR B/A	Port B/A Interrupt Request. High = active.

The programming address summary for the status, ports, and timer are as follows:

I/O Address	Number of Bits	Function
XXXXX000	8	Command Status
XXXXX001	8	PA
XXXXX010	8	PB
XXXXX011	6	PC
XXXXX100	8	Timer-Low
XXXXX101	8	Timer-High

TIMER

The Internal Timer is a 14-bit binary down counter capable of operating in 4 modes. Its desired mode of operation is programmable at any time during operation. Any TTL clock meeting timer in requirements (See AC Characteristics) may be used as a time base and fed to the timer input. The timer output may be looped around and cause an interrupt or used as I/O control. The operational modes are defined as follows and programmed along with the 6 high bits of timer data.

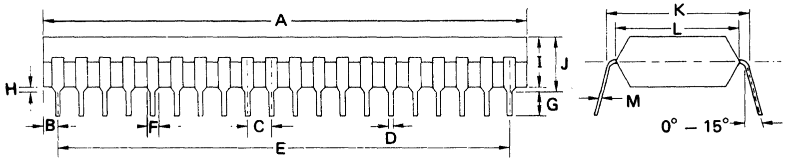
M2	M1	Operation
0	0	High at Start, Low During Second Half of Count
0	1	Square Wave (Period = Count Length, Auto Reload at TC)
1	0	Single Pulse at TC
1	1	Single Pulse at TC with Auto Reload

Programming the timer requires two words to be written to the μPD8155/8156 at I/O address XXXXX100 and XXXXX101 for the low and high order bytes respectively. Valid count length must be between 2_H and $3FFF_H$. The bit assignments for the high and low programming words are as follows:

Word	Bit Pattern								I/O Address
High Byte	M_2	M_1	T13	T12	T11	T10	T9	T8	XXXXX101
Low Byte	T7	T6	T5	T4	T3	T2	T1	T0	XXXXX100

The control of the timer is performed by TM2 and TM1 of the Command Status Word.

PACKAGE OUTLINE
μPD8155C
μPD8156C



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

NEC Microcomputers, Inc.

NEC

μPB8212

EIGHT-BIT INPUT/OUTPUT PORT

DESCRIPTION

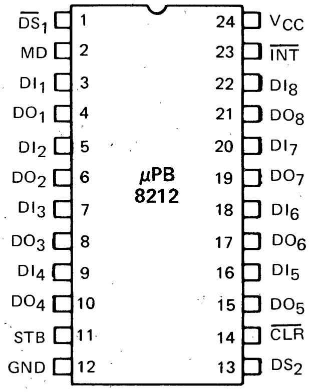
The μPB8212 input/output port consists of an 8-bit latch with three-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the control and generation of interrupts to the microprocessor.

The device is multimode in nature and can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

FEATURES

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current – 0.25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in 24-pin Plastic and Cerdip Packages

PIN CONFIGURATION



PIN NAMES

DI_1 – DI_8	Data In
DO_1 – DO_8	Data Out
$\overline{DS_1}$, DS_2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt (Active Low)
$\overline{CLR}$	Clear (Active Low)

FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that compose the data latch are of a "D" type design. The output (Q) of the flip-flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The output of the data latch (Q) are connected to three-state, non-inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three-state).

This high-impedance state allows the designer to connect the μPB8212 directly to the microprocessor bi-directional data bus.

Control Logic

The μPB8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

Service Request Flip-Flop (SR)

The (SR) flip-flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output (Q) of the (SR) flip-flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

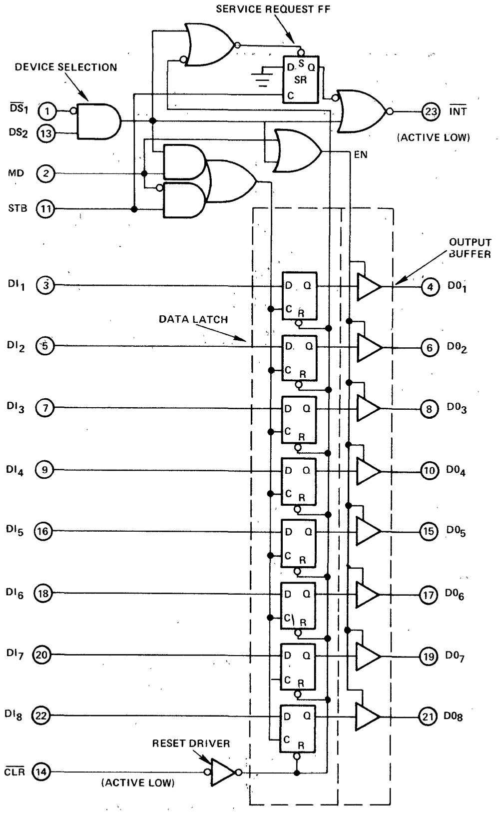
ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
All Output or Supply Voltages	–0.5 to +7 Volts
All Input Voltages	–1.0 to +5.5 Volts
Output Currents	125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

BLOCK DIAGRAM



STB	MD	$(\overline{DS}_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

$\overline{CLR}$	$(\overline{DS}_1 \cdot DS_2)$	STB	SR ②	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	0	0	③	③
1	↘	0	1	1
1	0	↘	0	0
1	1	0	1	0
1	1	↘	0	0

Notes: ① $\overline{CLR}$ resets data latch sets SR flip-flop. (No effect on output buffer)
② Internal SR flip-flop
③ Previous data remains

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$

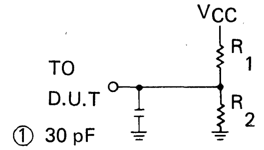
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	I_F		−0.14	−0.25	mA	$V_F = 0.45V$
Input Load Current MD Input	I_F		−0.25	−0.75	mA	$V_F = 0.45V$
Input Load Current $\overline{DS}_1$ Input	I_F		−0.26	−1.0	mA	$V_F = 0.45V$
Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	I_R			10	μA	$V_R = 5.25V$
Input Leakage Current MD Input	I_R			30	μA	$V_R = 5.25V$
Input Leakage Current $\overline{DS}_1$ Input	I_R			40	μA	$V_R = 5.25V$
Input Forward Voltage Clamp	V_C		−0.85	−1.3	V	$I_C = -5$ mA
Input "Low" Voltage	V_{IL}			0.85	V	
Input "High" Voltage	V_{IH}	2.0			V	
Output "Low" Voltage	V_{OL}		0.26	0.45	V	$I_{OL} = 15$ mA
Output "High" Voltage	V_{OH}	3.65	4.0		V	$I_{OH} = -1$ mA
Short Circuit Output Current	I_{SC}	−15	−38	−75	mA	$V_O = 0V$
Output Leakage Current High Impedance State	I_O			20	μA	$V_O = 0.45V/5.25V$
Power Supply Current	I_{CC}		103	130	mA	

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Pulse Width	t_{pw}	30			ns	Input Pulse Amplitude = 2.5V Input Rise and Fall Times = 5 ns Between 1V and 2V Measurement made at 1.5V with 15 mA and 30 pF Test Load
Data To Output Delay	t_{pd}		20	30	ns	
Write Enable To Output Delay	t_{we}			40	ns	
Data Setup Time	t_{set}	15			ns	
Data Hold Time	t_h	20			ns	
Reset to Output Delay	t_r			40	ns	
Set To Output Delay	t_s			30	ns	
Output Enable/Disable Time	t_e/t_d			45	ns	①
Clear To Output Delay	t_c			55	ns	②

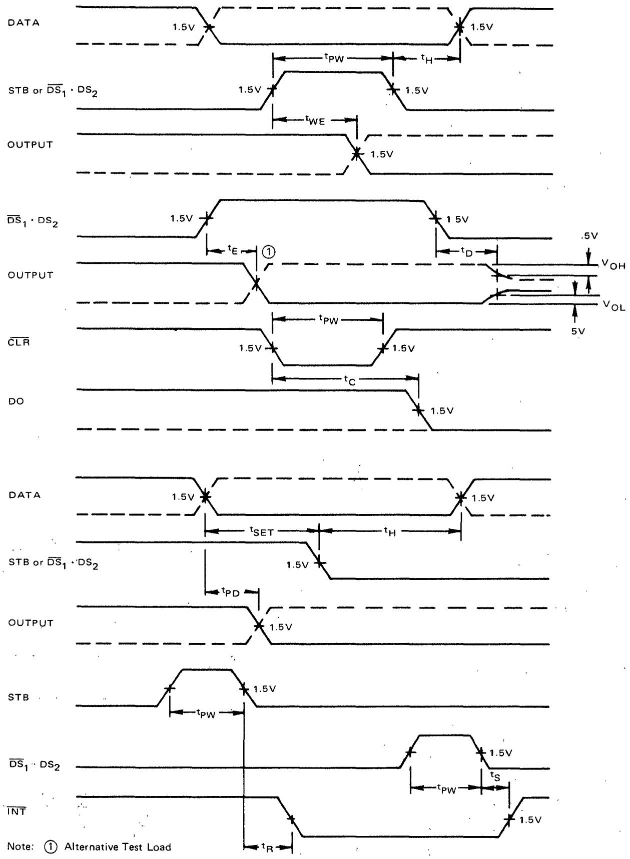
Notes: ① $R_1 = 300\Omega/10K\Omega$; $R_2 = 600\Omega/1K\Omega$
② $R_1 = 300\Omega$; $R_2 = 600\Omega$



TEST CIRCUIT

Note: ① Including Jig and Probe Capacitance

TIMING WAVEFORMS



Note: ① Alternative Test Load

CAPACITANCE ①

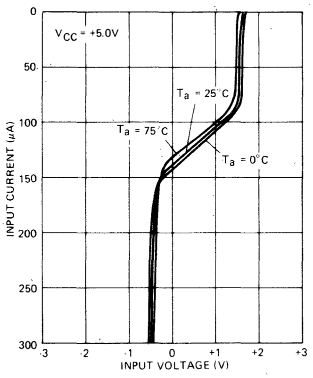
$T_a = 25°C$; $V_{CC} = +5V$; $V_{BIAS} = 2.5V$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}		7	12	pF	$\overline{DS_1}$, MD
Input Capacitance	C_{IN}		4	9	pF	DS_2, CLR, STB, $DI_1 - DI_8$
Output Capacitance	C_{OUT}		6	12	pF	$DO_1 - DO_8$

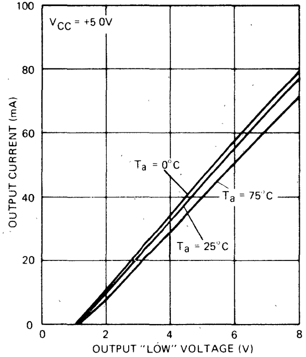
Note: ① This parameter is periodically sampled and not 100% tested

TYPICAL CHARACTERISTICS

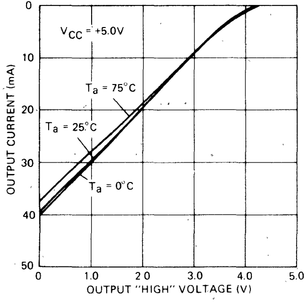
INPUT CURRENT VS. INPUT VOLTAGE



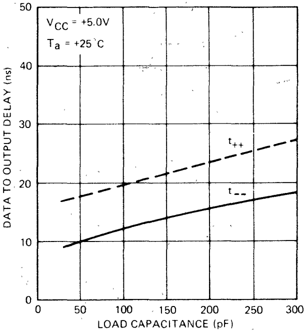
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



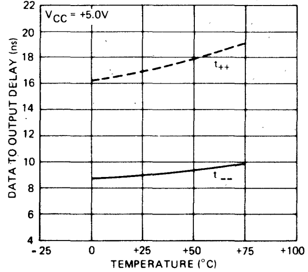
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



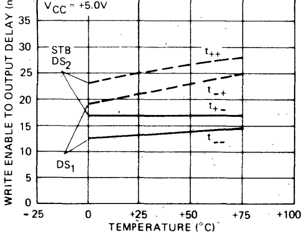
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



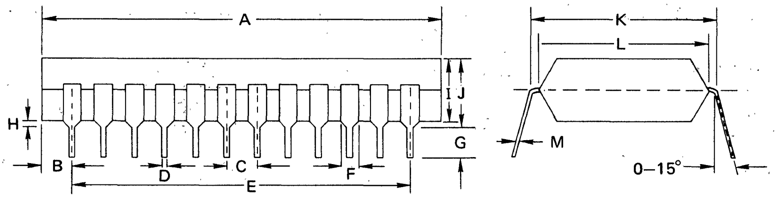
DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE

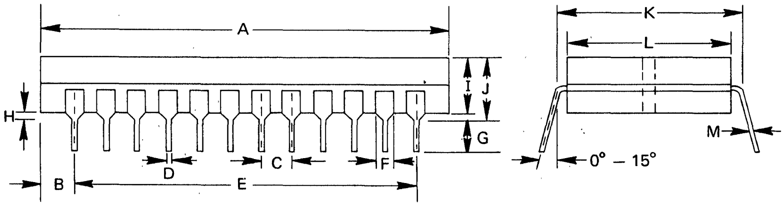


PACKAGE OUTLINE
μPB8212C/D



μPB8212C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPB8212D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

NEC Microcomputers, Inc.

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μPB8214

PRIORITY INTERRUPT CONTROLLER

DESCRIPTION

The μPB8214 is an eight-level priority interrupt controller. Designed to simplify interrupt driven microcomputer systems, the μPB8214 requires a single +5V power supply and is packaged in a 24 pin plastic Dual-in-line package.

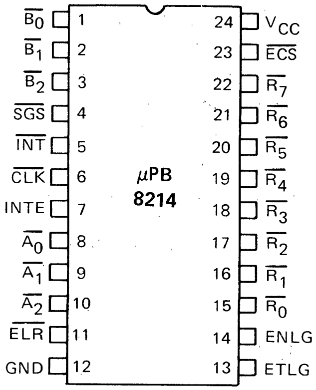
The μPB8214 accepts up to eight interrupts, determines which has the highest priority and then compares that priority with a software created current status register. If the incoming requires is of a higher priority than the interrupt currently being serviced, an interrupt request to the processor is generated. Vector information that identifies the interrupting device is also generated.

The interrupt structure of the microcomputer system can be expanded beyond eight interrupt levels by cascading μPB8214s. The μPB8214's interrupt and vector information outputs are open collector and control signals are provided to simplify expansion of the interrupt structure.

FEATURES

- Eight Priority Levels
- Current Status Register and Priority Comparator
- Easily Expanded Interrupt Structure
- Single +5 Volt Supply

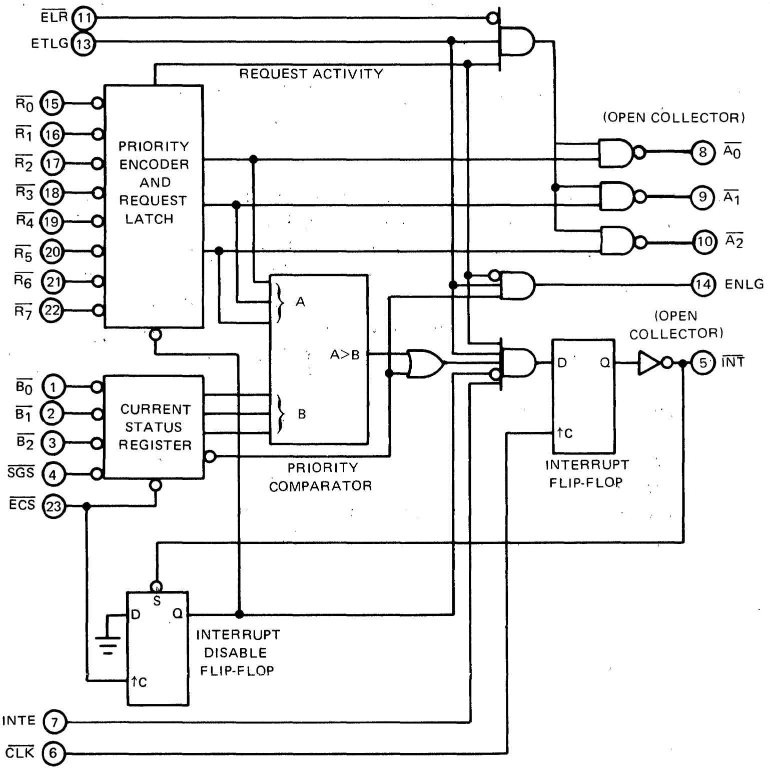
PIN CONFIGURATION



PIN NAMES

Inputs		
$\overline{R_0}$–$\overline{R_7}$	Request Levels ($\overline{R_7}$ Highest Priority)	
$\overline{B_0}$–$\overline{B_2}$	Current Status	
$\overline{SGS}$	Status Group Select	
$\overline{ECS}$	Enable Current Status	
INTE	Interrupt Enable	
$\overline{CLK}$	Clock (INT F-F)	
$\overline{ELR}$	Enable Level Read	
ETLG	Enable This Level Group	
Outputs		
$\overline{A_0}$–$\overline{A_2}$	Request Levels	Open Collector
$\overline{INT}$	Interrupt (Act Low)	
ENLG	Enable Next Level Group	

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General

The μPB8214 is an LSI device designed to simplify the circuitry required to implement an interrupt driven microcomputer system. Up to eight interrupting devices can be connected to a μPB8214, which will assign priority to incoming interrupt requests and accept the highest. It will also compare the priority of the highest incoming request with the priority of the interrupt being serviced. If the serviced interrupt has a higher priority, the incoming request will not be accepted.

A system with more than eight interrupting devices can be implemented by interconnecting additional μPB8214s. In order to facilitate this expansion, control signals are provided for cascading the controllers so that there is a priority established among the controllers. In addition, the interrupt and vector information outputs are open collector.

Priority Encoder and Request Latch

The priority encoder portion of the μPB8214 accepts up to eight active low interrupt requests ($\overline{R_0}$–$\overline{R_7}$). The circuit assigns priority to the incoming requests, with $\overline{R_7}$ having the highest priority and $\overline{R_0}$ the lowest. If two or more requests occur simultaneously, the μPB8214 accepts the one having the highest priority. Once an incoming interrupt request is accepted, it is stored by the request latch and a three-bit code is output. As shown in the following table, the outputs, ($\overline{A_0}$–$\overline{A_2}$) are the complement of the request level (modulo 8) and directly correspond to the bit pattern required to generate the one byte RESTART (RST) instructions recognized by an 8080A. Simultaneously with the $\overline{A_0}$–$\overline{A_2}$ outputs, a system interrupt request ($\overline{INT}$) is output by the μPB8214. It should be noted that incoming interrupt requests that are *not* accepted are not latched and must remain as an input to the μPB8214 in order to be serviced.

FUNCTIONAL DESCRIPTION (CONT.)

RESTART GENERATION TABLE

PRIORITY REQUEST		RST	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			1	1	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	1	1	1
LOWEST	$\overline{R_0}$	7	1	1	1	1	1	1	1	1
	$\overline{R_1}$	6	1	1	1	1	0	1	1	1
	$\overline{R_2}$	5	1	1	1	0	1	1	1	1
	$\overline{R_3}$	4	1	1	1	0	0	1	1	1
	$\overline{R_4}$	3	1	1	0	1	1	1	1	1
	$\overline{R_5}$	2	1	1	0	1	0	1	1	1
↓	$\overline{R_6}$	1	1	1	0	0	1	1	1	1
HIGHEST	$\overline{R_7}$	0*	1	1	0	0	0	1	1	1

*CAUTION: RST 0 will vector the program counter to location 0 (zero) and invoke the same routine as the "RESET" input to 8080A.

Current Status Register

The current status register is designed to prevent an incoming interrupt request from overriding the servicing of an interrupt with higher priority. Via software, the priority level of the interrupt being serviced by the microprocessor is written into the current status register on $\overline{B_0}$–$\overline{B_2}$. The bit pattern written should be the complement of the interrupt level.

The interrupt level currently being serviced is written into the current status register by driving $\overline{\text{ECS}}$ (Enable Current Status) low. The μPB8214 will only accept interrupts with a higher priority than the value contained by the current status register. Note that the programmer is free to use the current status register for other than as above. Other levels may be written into it. The comparison may be completely disabled by driving $\overline{\text{SGS}}$ (Status Group Select) low when $\overline{\text{ECS}}$ is driven low. This will cause the μPB8214 to accept incoming interrupts only on the basis of their priority to each other.

Priority Comparator

The priority comparator circuitry compares the level of the interrupt accepted by the priority encoder and request latch with the contents of the current status register. If the incoming request has a priority level higher than that of the current status register, the $\overline{\text{INT}}$ output is enabled. Note that this comparison can be disabled by loading the current status register with $\overline{\text{SGS}}$=0.

Expansion Control Signals

A microcomputer design may often require more than eight different interrupts. The μPB8214 is designed so that interrupt system expansion is easily performed via the use of three signals: ETLG (Enable This Level Group); ENLG (Enable Next Level Group); and $\overline{\text{ELR}}$ (Enable Level Read). A high input to ETLG indicates that the μPB8214 may accept an interrupt. In a typical system, the ENLG output from one μPB8214 is connected to the ETLG input of another μPB8214, etc. The ETLG of the μPB8214 with the highest priority is tied high. This configuration sets up priority among the cascaded μPB8214's. The ENLG output will be high for any device that does not have an interrupt pending, thereby allowing a device with lower priority to accept interrupts. The $\overline{\text{ELR}}$ input is basically a chip enable and allows hardware or software to selectively disable/enable individual μPB8214's. A low on the $\overline{\text{ELR}}$ input enables the device.

FUNCTIONAL DESCRIPTION (CONT.)

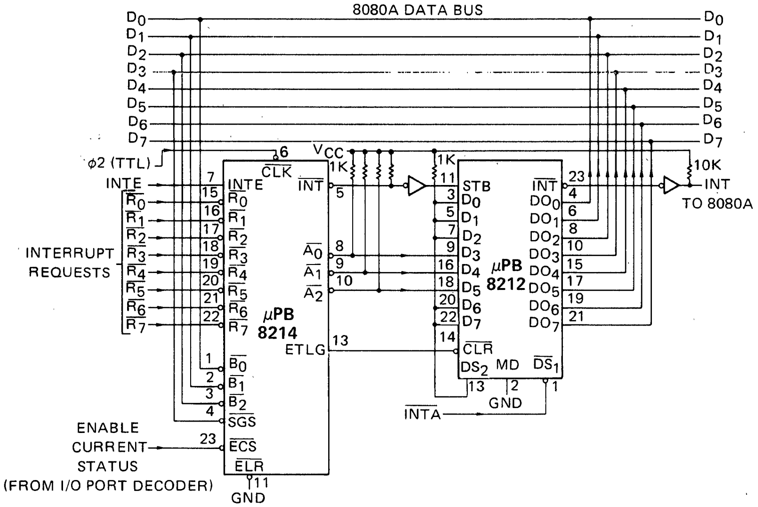
Interrupt Control Circuitry

The μPB8214 contains two flip-flops and several gates which determine whether an accepted interrupt request to the μPB8214 will generate a system interrupt to the 8080A. A condition gate drives the D input of the interrupt flip-flop whenever an interrupt request has been completely accepted. This requires that: the ETLG (Enable This Level Group) and INTE (Interrupt Enable) inputs to the μPB8214 are high; the $\overline{\text{ELR}}$ input is low; the incoming request must be of a higher priority than the contents of the current status register; and the μPB8214 must have been enabled to accept interrupt requests by the clearing of the interrupt disable flip-flop.

Once the condition gate drives the D input of the interrupt flip-flop high, a system interrupt ($\overline{\text{INT}}$) to the 8080A is generated on the next rising edge of the $\overline{\text{CLK}}$ input to the μPB8214. This $\overline{\text{CLK}}$ input is typically connected to the ϕ2 (TTL) output of an 8224 so that 8080A set-up time specifications are met. When $\overline{\text{INT}}$ is generated, it sets the interrupt disable flip-flop so that no additional system interrupts will be generated until it is reset. It is reset by driving $\overline{\text{ECS}}$ (Enable Current Status) low, thereby writing into the current status register.

It should be noted that the open collector $\overline{\text{INT}}$ output from the μPB8214 is active for only one clock period and thus must be externally latched for inputting to the 8080A. Also, because the $\overline{\text{INT}}$ output is open collector, when μPB8214's are cascaded, an $\overline{\text{INT}}$ output from any one will set all of the interrupt disable flip-flops in the array. Each μPB8214's interrupt disable flip-flop must then be cleared individually in order to generate subsequent system interrupts.

TYPICAL μPB8214 CIRCUITRY



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output and Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Clamp Voltage (all inputs)	V_C			−1.0	V	I_C=−5mA
Input Forward Current: ETLG input all other inputs	I_F		−.15 −.08	−0.5 −0.25	mA mA	V_F=0.45V
Input Reverse Current: ETLG input all other inputs	I_R			80 40	μA μA	V_R=5.25V
Input LOW Voltage: all inputs	V_{IL}			0.8	V	V_{CC}=5.0V
Input HIGH Voltage: all inputs	V_{IH}	2.0			V	V_{CC}=5.0V
Power Supply Current	I_{CC}		90	130	mA	②
Output LOW Voltage: all outputs	V_{OL}		.3	.45	V	I_{OL}=10mA
Output HIGH Voltage: ENLG output	V_{OH}	2.4	3.0		V	I_{OH}=−1mA
Short Circuit Output Current: ENLG output	I_{OS}	−20	−35	−55	mA	V_{OS}=0V, V_{CC}=5.0V
Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$–$\overline{A_2}$	I_{CEX}			100	μA	V_{CEX}=5.25V

CAPACITANCE ③

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	10	pF	V_{BIAS}=2.5V
Output Capacitance	C_{OUT}		7	12	pF	V_{CC}=5V f=1mHz

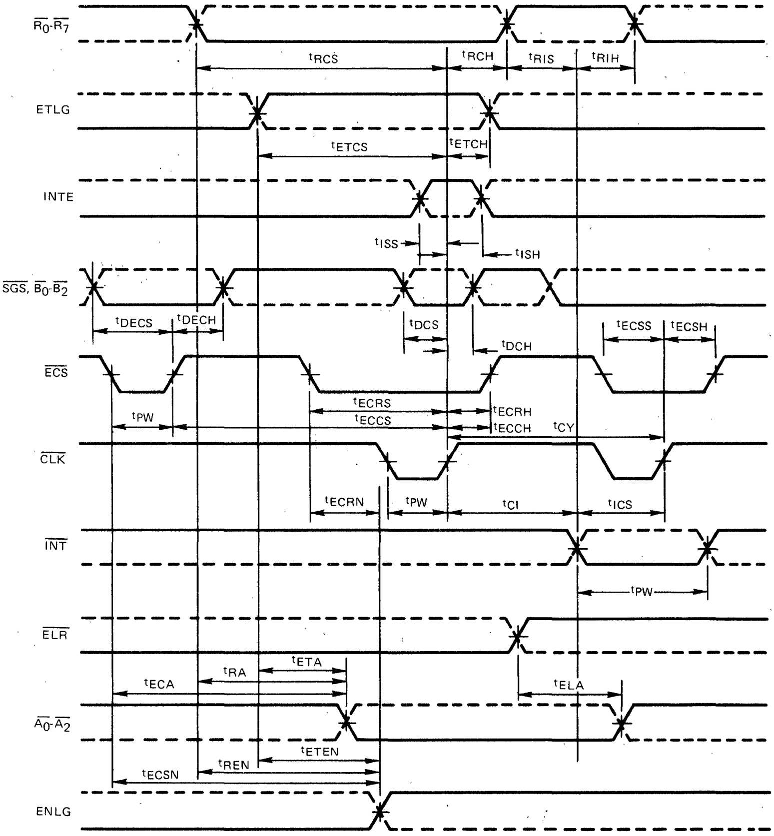
AC CHARACTERISTICS

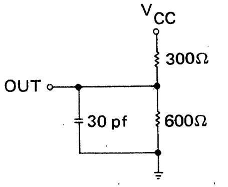
T_a = 0°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
$\overline{CLK}$ Cycle Time	t_{CY}	80	50		ns	Input pulse amplitude: 2.5 Volts
$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	t_{PW}	25	15		ns	
INTE Setup Time to $\overline{CLK}$	t_{ISS}	16	12		ns	
INTE Hold Time after $\overline{CLK}$	t_{ISH}	20	10		ns	
ETLG Setup Time to $\overline{CLK}$	t_{ETCS}④	25	12		ns	Input rise and fall times: 5 ns between 1 and 2 Volts
ETLG Hold Time After $\overline{CLK}$	t_{ETCH}④	20	10		ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECCS}④	80	50		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECCH}⑤	0			ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECRS}⑤	110	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECRH}⑤	0				Output loading of 15 mA and 30 pF.
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECSS}④	75	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECSH}④	0			ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{CLK}$	t_{DCS}④	70	50		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{CLK}$	t_{DCH}④	0			ns	Speed measurements taken at the 1.5 Volts levels.
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{CLK}$	t_{RCS}⑤	90	55		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{CLK}$	t_{RCH}⑤	0			ns	
$\overline{INT}$ Setup Time to $\overline{CLK}$	t_{ICS}	55	35		ns	
$\overline{CLK}$ to $\overline{INT}$ Propagation Delay	t_{CI}		15	25	ns	
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{INT}$	t_{RIS}⑥	10	0		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{INT}$	t_{RIH}⑥	35	20		ns	
$\overline{R_0}$–$\overline{R_7}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{RA}		80	100	ns	
$\overline{ELR}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ELA}		40	55	ns	
$\overline{ECS}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ECA}		100	120	ns	
ETLG to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ETA}		35	70	ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{ECS}$	t_{DECS}⑥	15	10		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{ECS}$	t_{DECH}⑥	15	10		ns	
$\overline{R_0}$–$\overline{R_7}$ to ENLG Propagation Delay	t_{REN}		45	70	ns	
ELTG to ENLG Propagation Delay	t_{ETEN}		20	25	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECRN}		85	90	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECSN}		35	55	ns	

Notes:
① Typical values are for T_a=25°C, V_{CC}=5.0V
② $\overline{B_0}$–$\overline{B_2}$, $\overline{SGS}$, $\overline{CLK}$, $\overline{R_0}$–$\overline{R_4}$ grounded, all other inputs and all outputs open.
③ This parameter is periodically sampled and not 100% tested.
④ Required for proper operation if INTE is enabled during next clock pulse.
⑤ These times are not required for proper operation but for desired change in interrupt flip-flop.
⑥ Required for new request or status to be properly loaded.

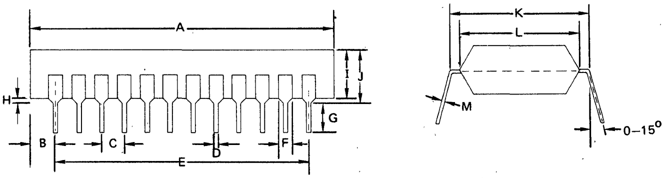
TIMING WAVEFORMS





TEST CIRCUIT

PACKAGE OUTLINE μPB8214C



ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.28
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	3.2 MIN.	0.125 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	0.25 ± 0.1	0.01 ± 0.004

SP8214-2-77-GN-CAT

NEC Microcomputers, Inc.

NEC

μPB8216
μPB8226

4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER

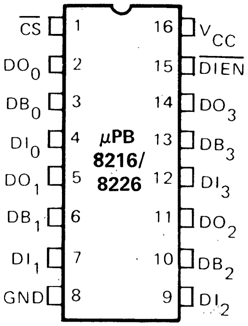
DESCRIPTION

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V (V_{OH}), and for high capacitance terminated bus structures, the DB outputs provide a high 55 mA (I_{OL}) capability.

FEATURES

- Data Bus Buffer Driver for μCOM-8 Microprocessor Family
- Low Input Load Current – 0.25 mA Maximum
- High Output Drive Capability for Driving System Data Bus
- 3.65V Output High Voltage for Direct Interface to μCOM-8 Microprocessor Family
- Three State Outputs
- Reduces System Package Count
- Available in 16 pin packages: Cerdip and Plastic

PIN CONFIGURATION



PIN NAMES

DB_0 - DB_3	Data Bus Bi Directional
DI_0 DI_3	Data Input
DO_0 – DO_3	Data Output
$\overline{DIEN}$	Data in Enable Direction Control
$\overline{CS}$	Chip Select

FUNCTIONAL DESCRIPTION

Microprocessors like the µPD8080A are MOS devices and are generally capable of driving a single TTL load. This also applies to MOS memory devices. This type of drive is sufficient for small systems with a few components, but often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The µPD8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers. They are three state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this is used to interface to the system side components such as memories, I/O, etc. Its interface is directly TTL compatible and it has high drive (55 mA). For maximum flexibility on the other side of the driver the inputs and outputs are separate. They can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080A Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080A processor is achieved with an adequate amount of noise immunity (650 mV worst case).

Control Gating $\overline{\text{CS}}$, $\overline{\text{DIEN}}$

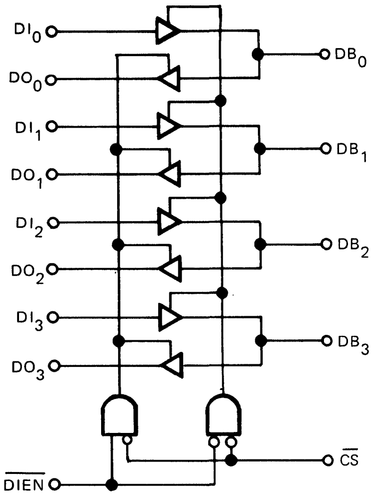
The $\overline{\text{CS}}$ input is used for device selection. When $\overline{\text{CS}}$ is "high" the output drivers are all forced to their high-impedance state. When it is "low" the device is selected (enabled) and the data flow direction is determined by the $\overline{\text{DIEN}}$ input.

The $\overline{\text{DIEN}}$ input controls the data flow direction (see Block Diagrams for complete truth table). This directional control is accomplished by forcing one of the pair of buffers to its high impedance state. This allows the other to transmit its data. This is accomplished by a simple two gate circuit.

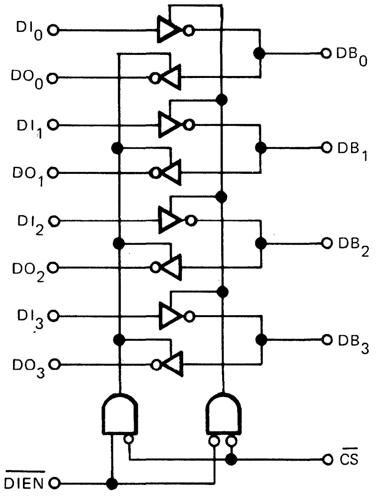
The µPB8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

BLOCK DIAGRAMS

8216



8226



$\overline{\text{DIEN}}$	$\overline{\text{CS}}$	RESULT
0	0	DI → DB
1	0	DB → DO
0	1	High Impedance
1	1	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to 70°C
Storage Temperature (Cerdip)	−65°C to +150°C
(Plastic)	−65°C to +125°C
All Output and Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.3 to +5.5 Volts
Output Currents	125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$^*T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP ①	MAX		
Input Load Current $\overline{\text{DIEN}}$, $\overline{\text{CS}}$		I_{F1}			−0.5	mA	$V_F = 0.45$
Input Load Current All Other Inputs		I_{F2}			−0.25	mA	$V_F = 0.45$
Input Leakage Current $\overline{\text{DIEN}}$, $\overline{\text{CS}}$		I_{R1}			20	μA	$V_R = 5.25V$
Input Leakage Current DI Inputs		I_{R2}			10	μA	$V_R = 5.25V$
Input Forward Voltage Clamp		V_C			−1.0	V	$I_C = -5$ mA
Input "Low" Voltage		V_{IL}			0.95	V	
Input "High" Voltage		V_{IH}	2.0			V	
Output Leakage Current (3-State)	DO	I_O			20	μA	$V_O = 0.45/5.25V$
	DB	I_O			100		
Power Supply Current	8216	I_{CC}			130	mA	
	8226	I_{CC}			120	mA	
Output "Low" Voltage		V_{OL1}			0.48	V	DO Outputs $I_{OL} = 15$ mA DB Outputs $I_{OL} = 25$ mA
Output "Low" Voltage	8216	V_{OL2}			0.7	V	DB Outputs $I_{OL} = 55$ mA
	8226	V_{OL2}			0.7	V	DB Outputs $I_{OH} = 50$ mA
Output "High" Voltage		V_{OH1}	3.65			V	DO Outputs $I_{OH} = -1$ mA
Output "High" Voltage		V_{OH2}	2.4			V	DB Outputs $I_{OH} = -10$ mA
Output Short Circuit Current		I_{OS}	−15		−65	mA	DO Outputs $V_O = 0V$
		I_{OS}	−30		−120	mA	DB Outputs $V_{CC} = 5.0V$

Note: ① Typical values are for $T_a = 25°C$, $V_{CC} = 5.0V$.

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			8	pF	$V_{BIAS} = 2.5V$ $V_{CC} = 5V$ $T_a = 25°C$ f = 1 MHz
Output Capacitance	C_{OUT1}			10 ②	pF	
Output Capacitance	C_{OUT2}			18 ③	pF	

Notes: ① This parameter is periodically sampled and not 100% tested.
② DO Output.
③ DB Output.

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V±5%

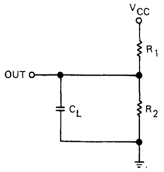
PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP ①	MAX		
Input to Output Delay DO Outputs		t_{PD1}			25	ns	C_L = 30 pF, R_1 = 300Ω, R_2 = 600Ω ④
Input to Output Delay DB Outputs	8216	t_{PD2}			30	ns	C_L = 300 pF, R_1 = 90Ω, R_2 = 180Ω 4
	8226	t_{PD2}			25	ns	
Output Enable Time	8216	t_E			65	ns	② ④
	8226	t_E			54	ns	
Output Disable Time		t_D			35	ns	③ ④

Notes: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V

② DO Outputs, C_L = 30 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 300 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

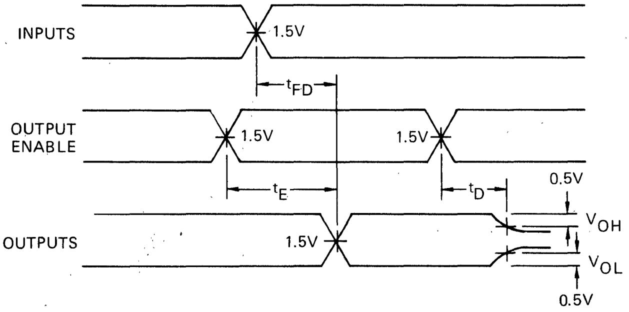
③ DO Outputs, C_L = 5 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 5 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

④ Input pulse amplitude: 2.5V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

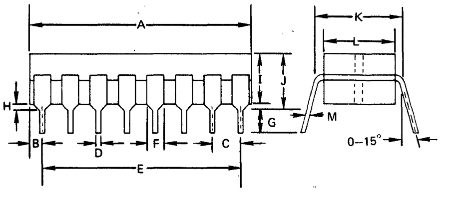


TEST CIRCUIT

TIMING WAVEFORMS

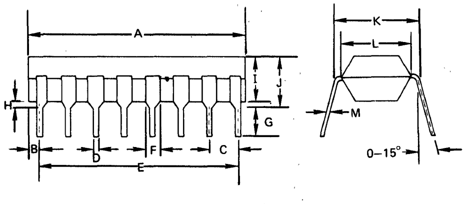


PACKAGE OUTLINE μPB8216C/D μPB8226C/D



Cerdip

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1 5	0.059
G	2.54 MIN	0.10 MIN
H	0 5 MIN	0.019 MIN
I	4.58 MAX	0 181 MAX
J	5.08 MAX	0 20 MAX
K	7 62	0.30
L	6.4	0.25
M	$0\ 25^{+0.10}_{\ \ 0.05}$	$0\ 0098^{+0\ 0039}_{\ \ 0.0019}$



Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0 76 MAX
B	0 81	0 03
C	2 54	0.10
D	0 5	0 02
E	17 78	0.70
F	1 3	0.051
G	2 54 MIN	0.10 MIN
H	0.5 MIN	0 02 MIN
I	4 05 MAX	0 16 MAX
J	4 55 MAX	0 18 MAX
K	7 62	0 30
L	6.4	0 25
M	$0\ 25^{+0\ 10}_{\ \ 0\ 05}$	0 01

SP8216/8226-8-77-GN-CAT

NEC Microcomputers, Inc.

NEC

μPB8224

CLOCK GENERATOR AND DRIVER FOR 8080A PROCESSORS

DESCRIPTION

The μPB8224 is a single chip clock generator and driver for 8080A processors. The clock frequency is determined by a user specified crystal and is capable of meeting the timing requirements of the entire 8080A family of processors. MOS and TTL level clock outputs are generated.

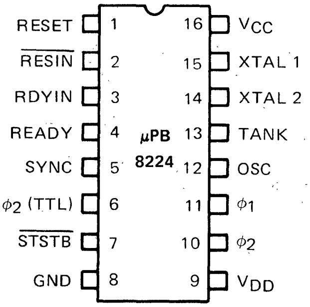
Additional logic circuitry of the μPB8224 provides signals for power-up reset, an advance status strobe and properly synchronizes the ready signal to the processor. This greatly reduces the number of chips needed for 8080A systems.

The μPB8224 is fabricated using NEC's Schottky bipolar process.

FEATURES

- Crystal Controlled Clocks
- Oscillator Output for External Timing
- MOS Level Clocks for 8080A Processor
- TTL Level Clock for DMA Activities
- Power-up Reset for 8080A Processor
- Ready Synchronization
- Advanced Status Strobe
- Reduces System Package Count
- Available in 16-pin Cerdip and Plastic Packages

PIN CONFIGURATION



PIN NAMES

$\overline{\text{RESIN}}$	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
$\overline{\text{STSTB}}$	Status STB Output
φ1	Processor Clocks
φ2	
XTAL 1	Crystal Connections
XTAL 2	
TANK	Used With Overtone Crystal
OSC	Oscillator Output
φ2 (TTL)	φ2 CLK (TTL Level)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

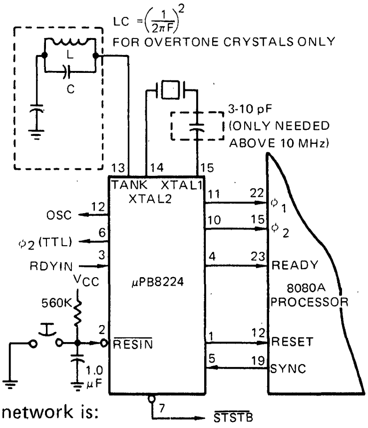
Clock Generator

The clock generator circuitry consists of a crystal controlled oscillator and a divide-by-nine counter. The crystal frequency is a function of the 8080A processor speed and is basically nine times the processor frequency, i.e.:

$$\text{Crystal frequency} = \frac{9}{t_{CY}}$$

where t_{CY} is the 8080A processor clock period.

A series resonant fundamental mode crystal is normally used and is connected across input pins XTAL1 and XTAL2. If an overtone mode crystal is used, an additional LC network, AC coupled to ground, must be connected to the TANK input of the μPB8224 as shown in the following figure.



The formula for the LC network is:

$$LC = \left(\frac{1}{2\pi F}\right)^2$$

where F is the desired frequency of oscillation.

The output of the oscillator is input to the divide-by-nine counter. It is also buffered and brought out on the OSC pin, allowing this stable, crystal controlled source to be used for derivation of other system timing signals. The divide-by-nine counter generates the two non-overlapping processor clocks, ϕ_1 and ϕ_2, which are buffered and at MOS levels, a TTL level ϕ_2 and internal timing signals.

The ϕ_1 and ϕ_2 high level outputs are generated in a 2-5-2 digital pattern, with ϕ_1 being high for two oscillator periods, ϕ_2 being high for five oscillator periods, and then neither being high for two oscillator periods. The TTL level ϕ_2, ϕ_2 (TTL), is normally used for DMA activities by gating the external device onto the 8080A bus once a Hold Acknowledge (HLDA) has been issued.

Additional Logic

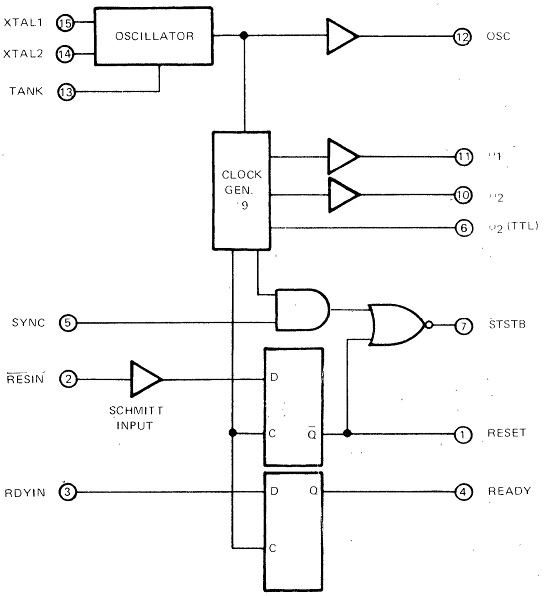
In addition to the clock generator circuitry, the μPB8224 contains additional logic to aid the system designer in the proper timing of several interface signals.

The $\overline{\text{STSTB}}$ signal indicates, at the earliest possible moment, when the status signals output from the 8080A processor are stable on the data bus. $\overline{\text{STSTB}}$ is designed to connect directly to the μPB8228 System Controller and automatically resets the μPB8228 during power-on Reset.

The $\overline{\text{RESIN}}$ input to the μPB8224 is used to automatically generate a RESET signal to the 8080A during power initialization. The slow rise of the power supply voltage in an external RC network is sensed by an internal Schmitt Trigger. The output of the Schmitt Trigger is gated to generate an 8080A compatible RESET. An active low manual switch may also be attached to the RC circuit for manual system reset.

The RDYIN input to the μPB8224 accepts an asynchronous "wait request" and generates a READY output to the 8080A that is fully synchronized to meet the 8080A timing requirements.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output Voltages (TTL)	−0.5 to +7 Volts
All Output Voltages (MOS)	−1.0 to +13.5 Volts
All Input Voltages	−1.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts
Supply Voltage V_{DD}	−0.5 to +13.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Current Loading	I_F			-0.25	mA	$V_F = 0.45V$
Input Leakage Current	I_R			10	μA	$V_R = 5.25V$
Input Forward Clamp Voltage	V_C			-1.0	V	$I_C = -5$ mA
Input "Low" Voltage	V_{IL}			0.8	V	$V_{CC} = 5.0V$
Input "High" Voltage	V_{IH}	2.6			V	Reset Input
		2.0				All Other Inputs
$\overline{RESIN}$ Input Hysteresis	V_{IH}-V_{IL}	0.25			V	$V_{CC} = 5.0V$
Output "Low" Voltage	V_{OL}			0.45	V	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ $I_{OL} = 2.5$ mA
				0.45	V	All Other Inputs $I_{OL} = 15$ mA
Output "High" Voltage	V_{OH}					
ϕ_1, ϕ_2		9.4			V	$I_{OH} = -100$ μA
READY, RESET		3.6			V	$I_{OH} = -100$ μA
All Other Outputs		2.4			V	$I_{OH} = -1$ mA
Output Short Circuit Current (All Low Voltage Outputs Only)	I_{SC} ①	-10		-60	mA	$V_O = 0V$ $V_{CC} = 5.0V$
Power Supply Current	I_{CC}			115	mA	
Power Supply Current	I_{DD}			15	mA	

Note: ① Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CAPACITANCE①

$T_a = 25°C$; f = 1 MHz; $V_{CC} = 5V$; $V_{DD} = 12V$; $V_{BIAS} = 2.5V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			8	pF	

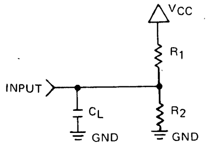
Note: ① This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$; $V_{DD} = +12V \pm 5\%$

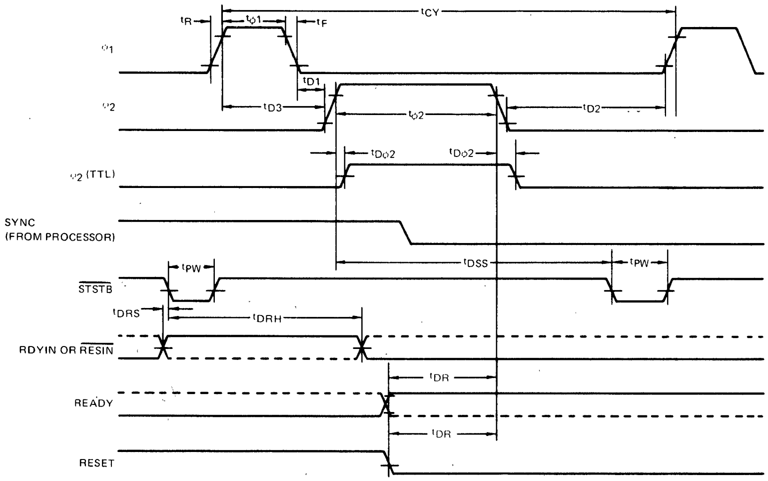
PARAMETER	SYMBOL	LIMITS ①			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
ϕ_1 Pulse Width	$t_{\phi 1}$	$\frac{2t_{CY}}{9} - 20$ ns			ns	$C_L = 20$ pF to 50 pF
ϕ_2 Pulse Width	$t_{\phi 2}$	$\frac{5t_{CY}}{9} - 35$ ns				
ϕ_1 to ϕ_2 Delay	t_{D1}	0				
ϕ_2 to ϕ_1 Delay	t_{D2}	$\frac{2t_{CY}}{9} - 14$ ns				
ϕ_1 to ϕ_2 Delay	t_{D3}	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20$ ns		
ϕ_1 and ϕ_2 Rise Time	t_R			20		
ϕ_1 and ϕ_2 Fall Time	t_F			20		
ϕ_2 to ϕ_2 (TTL) Delay	$t_{D\phi 2}$	−5		+15	ns	ϕ_2 TTL, CL = 30 pF $R_1 = 300\Omega$ $R_2 = 600\Omega$
ϕ_2 to $\overline{\text{STSTB}}$ Delay	t_{DSS}	$\frac{6t_{CY}}{9} - 30$ ns		$\frac{6t_{CY}}{9}$	ns	$\overline{\text{STSTB}}$, CL = 15 pF $R_1 = 2K$ $R_2 = 4K$
$\overline{\text{STSTB}}$ Pulse Width	t_{PW}	$\frac{t_{CY}}{9} - 15$ ns			ns	
RDYIN Setup Time to $\overline{\text{STSTB}}$	t_{DRS}	$50 \text{ ns} - \frac{4t_{CY}}{9}$				
RDYIN Hold Time After $\overline{\text{STSB}}$	t_{DRH}	$\frac{4t_{CY}}{9}$				
READY or RESET to ϕ_2 Delay	t_{DR}	$\frac{4t_{CY}}{9} - 25$ ns			ns	Ready and Reset CL = 10 pF $R_1 = 2K$ $R_2 = 4K$
Crystal Frequency	f_{CLK}		$\frac{9}{t_{CY}}$		MHz	
Maximum Oscillating Frequency	f_{MAX}			27	MHz	

Note: ① t_{CY} represents the processor clock period



TEST CIRCUIT

TIMING WAVEFORMS



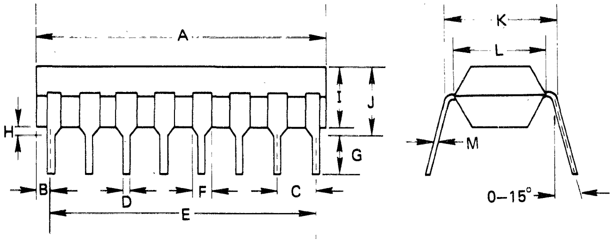
Voltage Measurement Points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

CRYSTAL REQUIREMENTS

Tolerance	0.005% at 0°C–70°C
Resonance	Series (Fundamental) ①
Load Capacitance	20-35 pF
Equivalent Resistance	75-20 ohms
Power Dissipation (Min)	4 mW

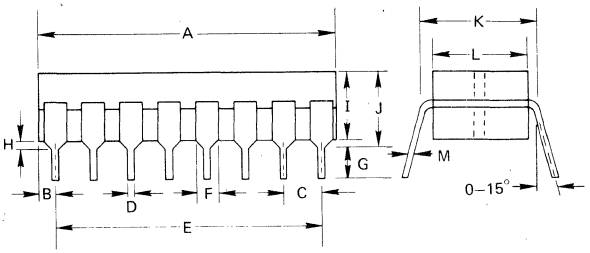
Note: ① With tank circuit use 3rd overtone mode.

PACKAGE OUTLINE μPB8224C/D



μPB8224C (Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01



μPB8224D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0 10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0 70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.8	0.27
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

NEC Microcomputers, Inc.

NEC
μPB8228
μPB8238

8080A SYSTEM CONTROLLER AND BUS DRIVER

DESCRIPTION

The μPB8228/8238 is a single chip controller and bus driver for 8080A based systems. All the required interface signals necessary to connect RAM, ROM and I/O components to a μPD8080A are generated.

The μPB8228/8238 provides a bi-directional three-state bus driver for high TTL fan-out and isolation of the processor data bus from the system data bus for increased noise immunity.

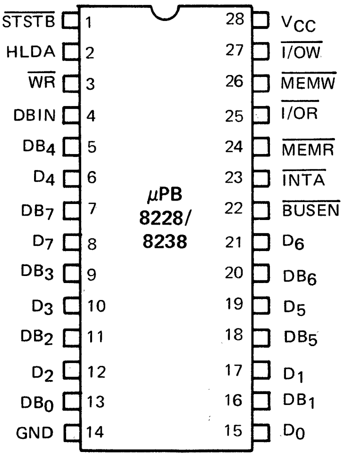
The system controller portion of the μPB8228/8238 consists of a status latch for definition of processor machine cycles and a gating array to decode this information for direct interface to system components. The controller can enable gating of a multi-byte interrupt onto the data bus or can automatically insert a RESTART 7 onto the data bus without any additional components.

Two devices are provided. The μPB8228 for small systems without tight write timing constraints and the μPB8238 for larger systems.

FEATURES

- System Controller for 8080A Systems
- Bi-Directional Data Bus for Processor Isolation
- 3.60V Output High Voltage for Direct Interface to 8080A Processor
- Three State Outputs on System Data Bus
- Enables Use of Multi-Byte Interrupt Instructions
- Generates RST 7 Interrupt Instruction
- μPB8228 for Small Memory Systems
- μPB8238 for Large Memory Systems
- Reduces System Package Count
- Schottky Bipolar Technology

PIN CONFIGURATION



NC: No Connection

PIN NAMES

$D_7 - D_0$	Data Bus (Processor Side)
$DB_7 - DB_0$	Data Bus (System Side)
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
DBIN	DBIN (From Processor)
$\overline{INTA}$	Interrupt Acknowledge
HLDA	HLDA (From Processor)
$\overline{WR}$	WR (From Processor)
$\overline{BUSEN}$	Bus Enable Input
$\overline{STSTB}$	Status Strobe (From μPB8224)
V_{CC}	+5V
GND	0 Volts

Rev/1

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver

The eight bit, bi-directional bus driver provides buffering between the processor data bus and the system data bus. On the processor side, the μPB8228/8238 exceeds the minimum input voltage requirements (3.0V) of the μPD8080A. On the system side, the driver is capable of adequate drive current (10 mA) for connection of a large number of memory and I/O devices to the bus. Signal flow in the bus driver is controlled by the gating array and its outputs can be forced into a high impedance state by use of the BUSEN input.

Status Latch

The Status Latch in the μPB8228/8238 stores the status information placed on the data bus by the 8080A at the beginning of each machine cycle. The information is latched when STSTB goes low and is then decoded by the gating array for the generation of control signals.

Gating Array

The Gating Array generates "active low" control signals for direct interfacing to system components by gating the contents of the status latch with control signals from the 8080A.

MEM/R, I/OR and INTA are generated by gating the DBIN signal from the processor with the contents of the status latch. I/OR is used to enable an I/O input onto the system data bus. MEM/R is used to enable a memory input.

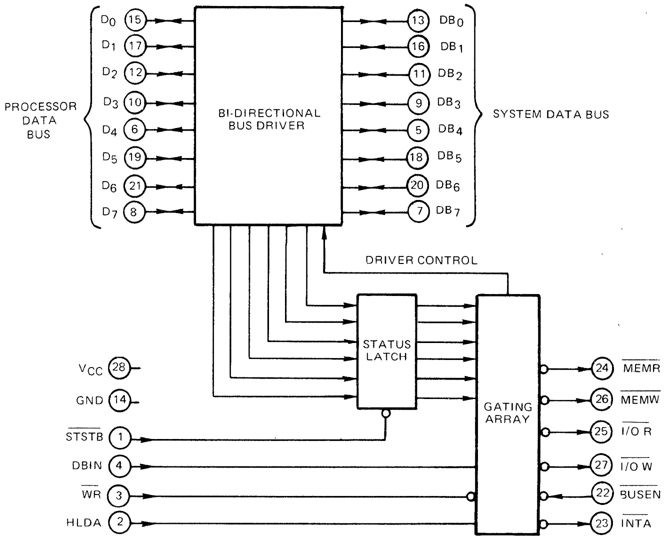
INTA is normally used to gate an interrupt instruction onto the system data bus. When used with the μPD8080A processor, the μPB8228/8238 will decode an interrupt acknowledge status word during all three machine cycles for a multi-byte interrupt instruction. For 8080A type processors that do not generate an interrupt acknowledge status word during the second and third machine cycles of a multi-byte interrupt instruction, the μPB8228/8238 will internally generate an INTA pulse for those machine cycles.

The μPB8228/8238 also provides the designer the ability to place a single interrupt instruction onto the bus without adding additional components. By connecting the +12 volt supply to the INTA output (pin 23) of the μPB8228/8238 through a 1 K ohm series resistor, RESTART 7 will be gated onto the processor data bus when DBIN is active during an interrupt acknowledge machine cycle.

MEM/W and I/OW are generated by gating the WR signal from the processor with the contents of the status latch. I/OW indicates that an output port write is about to occur. MEM/W indicates that a memory write will occur.

The data bus output buffers and control signal buffers can be asynchronously forced into a high impedance state by placing a high on the BUSEN pin of the μPB8228/8238. Normal operation is performed with BUSEN low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.5 to 5.5 Volts
Output Currents	100 mA

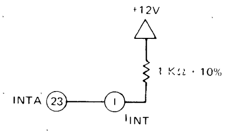
COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Clamp Voltage, All Inputs	V_C			-1.0	V	V_{CC} = 4.75V; I_{CC} = −5 mA
Input Load Current, $\overline{STSTB}$	I_F			500	µA	V_{CC} = 5.25V V_F = 0.45V
D_2 and D_6				750	µA	
D_0, D_1, D_4, D_5, and D_7				250	µA	
All Other Inputs				250	µA	
Input Leakage Current, $\overline{STSTB}$	I_R			100	µA	V_{CC} = 5.25V V_R = 5.0V
DB_0 through DB_7				20	µA	
All Other Inputs				100	µA	
Input Threshold Voltage, All Inputs	V_{TH}	0.8		2.0	V	V_{CC} = 5V
Power Supply Current	I_{CC}			190	mA	V_{CC} = 5.25V
Output Low Voltage, D_0 through D_7	V_{OL}			0.45	V	V_{CC} = 4.75V; I_{OL} = 2 mA
All Other Outputs				0.48	V	I_{OL} = 10 mA
Output High Voltage, D_0 through D_7	V_{OH}	3.6			V	V_{CC} = 4.75V; I_{OH} = −10 µA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Short Circuit Current, All Outputs	I_{OS}	15		90	mA	V_{CC} = 5V
Off State Output Current, All Control Outputs	$I_{O(off)}$			100	µA	V_{CC} = 5.25V; V_O = 5.0V
				-100	µA	V_O = 0.45V
INTA Current	I_{INT}			5	mA	(See Figure below)



INTA TEST CIRCUIT

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			12	pF	V_{BIAS} = 2.5V, V_{CC} = 5.0V, f = 1 MHz
Output Capacitance Control Signals	C_{OUT}			15	pF	
I/O Capacitance (D or DB)	$C_{I/O}$			15	pF	

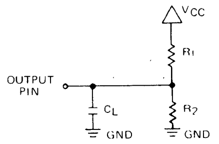
NOTE: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

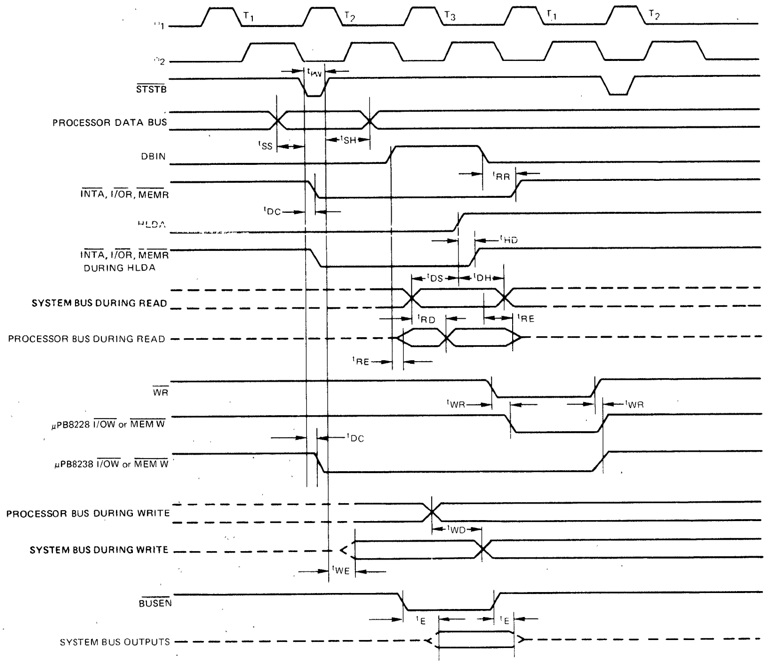
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Width of Status Strobe	t_{PW}	22			ns	
Setup Time, Status Inputs D_0-D_7	t_{SS}	8			ns	
Hold Time, Status Inputs D_0-D_7	t_{SH}	5			ns	
Delay from $\overline{STSTB}$ to any Control Signal	t_{DC}	20		60	ns	C_L = 100 pF
Delay from DBIN to Control Outputs	t_{RR}			30	ns	C_L = 100 pF
Delay from DBIN to Enable/Disable 8080A Bus	t_{RE}			45	ns	C_L = 25 pF
Delay from System Bus to 8080A Bus during Read	t_{RD}			30	ns	C_L = 25 pF
Delay from $\overline{WR}$ to Control Outputs	t_{WR}	5		45	ns	C_L = 100 pF
Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$	t_{WE}			30	ns	C_L = 100 pF
Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	t_{WD}	5		40	ns	C_L = 100 pF
Delay from $\overline{\text{System Bus Enable}}$ to System Bus DB_0-DB_7	t_E			30	ns	C_L = 100 pF
HLDA to Read Status Outputs	t_{HD}			25	ns	
Setup Time, System Bus Inputs to HLDA	t_{DS}	10			ns	
Hold Time, System Bus Inputs to HLDA	t_{DH}	20			ns	C_L = 100 pF

For D_0-D_7: R_1 = 4 KΩ, R_2 = ∞Ω, C_L = 25 pF. For all other outputs R_1 = 500Ω, R_2 = 1 KΩ, C_L = 100 pF.



TEST CIRCUIT

TIMING WAVEFORMS



VOLTAGE MEASUREMENT POINTS D_0-D_7 (when outputs) Logic "0" 0.8V, Logic "1" 3.0V. All other signals measured at 1.5V

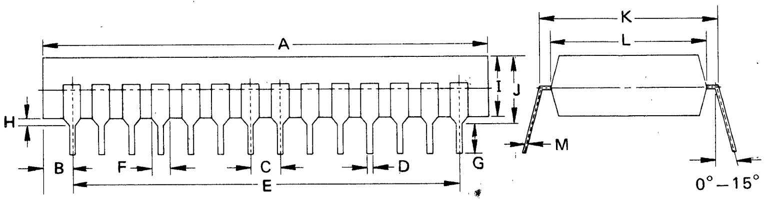
STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH ①	MEMORY READ ②	MEMORY WRITE ③	STACK READ ④	STACK WRITE ⑤	INPUT READ ⑥	OUTPUT WRITE ⑦	INTERRUPT ACKNOWLEDGE (M_1) ⑧	INT. ACK. (M_2, M_3) ⑨	HALT ACKNOWLEDGE ⑩	
D_0	INTA	0	0	0	0	0	0	0	1	0	1	µPD8080A OUTPUT
D_1	$\overline{\text{WO}}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEMR	1	1	0	1	0	0	0	0	1	0	
PIN NO.												
24	$\overline{\text{MEMR}}$	0	0	1	0	1	1	1	1	1	1	µPB8228/8238 OUTPUT
26	$\overline{\text{MEMW}}$	1	1	0	1	0	1	1	1	1	1	
25	$\overline{\text{I/OR}}$	1	1	1	1	1	0	1	1	1	1	
27	$\overline{\text{I/OW}}$	1	1	1	1	1	1	0	1	1	1	
23	$\overline{\text{INTA}}$	1	1	1	1	1	1	1	0	0	1	

SIGNAL STATUS

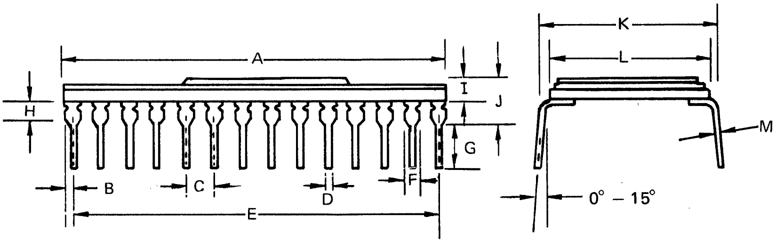
µPB8228/8238 CONTROL SIGNALS

PACKAGE OUTLINE
μPB8228C/D
μPB8238C/D



μPB8228/8238C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



μPB8228/8238D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.0 MAX	1.41 MAX.
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

SP8228/38-9-77-GN-CAT

NEC Microcomputers, Inc.

NEC
µPD8243

INPUT/OUTPUT EXPANDER FOR µPD8048/8748/8035

DESCRIPTION

The µPD8243 input/output expander is directly compatible with the µPD8048 family of single-chip microcomputers. Using NMOS technology the µPD8243 provides high drive capabilities while requiring only a single +5V supply voltage.

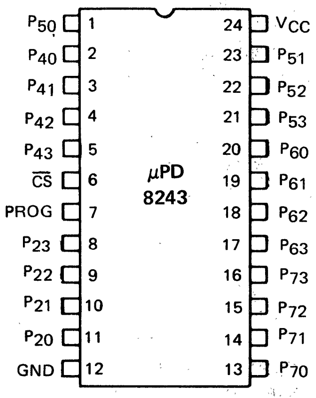
The µPD8243 interfaces to the µPD8048 family through a 4-bit I/O port and offers four 4-bit bi-directional static I/O ports. The ease of expansion allows for multiple µPD8243's to be added using the bus port.

The bi-directional I/O ports of the µPD8243 act as an extension of the I/O capabilities of the µPD8048 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

FEATURES

- Four 4-Bit I/O Ports
- Fully Compatible with µPD8048 Microcomputer Family
- High Output Drive
- NMOS Technology
- Single +5V Supply
- Direct Extension of Resident µPD8048 I/O Ports
- Logical AND and OR Directly to Ports
- Compatible with Industry Standard 8243
- Available in 24-Pin Plastic and Ceramic Packages

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

General Operation

The I/O capabilities of the μPD8048/8748/8035 can be enhanced in four 4-bit I/O port increments using one or more μPD8243's. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND Accumulator to Port.
- Logical OR Accumulator to Port.
- Transfer Port to Accumulator.
- Transfer Accumulator to Port.

Port 2 (P_{20}-P_{23}) forms the 4-bit bus through which the μPD8243 communicates with the host processor. The PROG output from the μPD8048/8748/8035 provides the necessary timing to the μPD8243. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the op-code and port address followed by the second nibble containing the 4-bit data. Multiple μPD8243's can be used for additional I/O. The output lines from the μPD8048/8748/8035 can be used to form the chip selects for the additional μPD8243's.

Power On Initialization

Applying power to the μPD8243 sets ports 4-7 to the tri-state mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high-to-low transition in order to exit from the power on mode. The power on sequence is initiated any time V_{CC} drops below 1V. The table below shows how the 4-bit nibbles on Port 2 correspond to the μPD8243 operations.

Port Address			Op-Code		
P_{21}	P_{20}	Address Code	P_{23}	P_{22}	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

For example an 0010 appearing on P_{20}-P_{23}, respectively, would result in a Write to Port 4.

Read Mode

There is one Read mode in the μPD8243. A falling edge on the PROG pin latches the op-code and port address from input Port 2. The port address and Read operation are then decoded causing the appropriate outputs to be tri-stated and the input buffers switched on. The rising edge of PROG terminates the Read operation. The Port (4,5,6, or 7) that was selected by the Port address (P_{21}-P_{20}) is returned to the tri-state mode, and Port 2 is switched to the input mode.

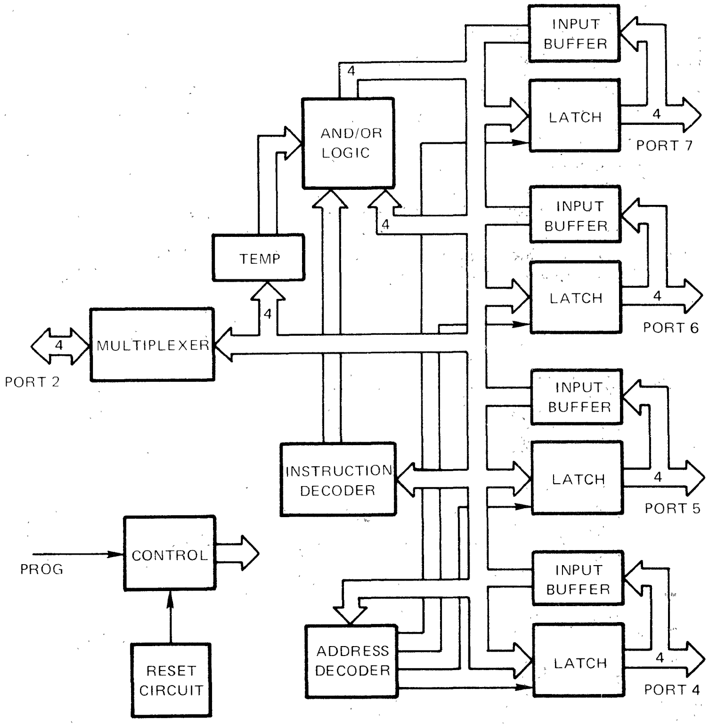
Generally, in the read mode, a port will be an input and in the write mode it will be an output. If during program operation, the μPD8243's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

Write Modes

There are three write modes in the μPD8243. The MOVD P_p,A instruction from the μPD8048/8748/8035 writes the new data directly to the specified port (4,5,6, or 7). The old data previously latched at that port is lost. The ORLD Pp,A instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD Pp,A instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN		FUNCTION
NO.	SYMBOL	
2-5 1, 21-23 17-20 13-16	P_{40}-P_{43} P_{50}-P_{53} P_{60}-P_{63} P_{70}-P_{73}	The four 4-bit static bi-directional I/O ports. They are programmable into the following modes: input mode (during a Read operation); low impedance latched output mode (after a Write operation); and the tri-state mode (following a Read operation). Data appearing on I/O lines P_{20}-P_{23} can be written directly. That data can also be logically ANDed or ORed with the previous data on those lines.
6	$\overline{CS}$	Chip Select input (active-low). When the µPD8343 is deselected ($\overline{CS}$ = 1), output or internal status changes are inhibited.
7	PROG	Clock input pin. The control and address information are present on port lines P_{20}-P_{23} when PROG makes a high-to-low transition. Data is present on port lines P_{20}-P_{23} when PROG makes a low-to-high transition.
8-11	P_{20}-P_{23}	P_{20}-P_{23} form a 4-bit bi-directional port. Refer to PROG function for contents of P_{20}-P_{23} at the rising and falling edges of PROG. Data from a selected port is present on P_{20}-P_{23} prior to the rising edge of PROG if during a Read operation.
12	GND	The µPD8041/8741 ground potential.
24	V_{CC}	+5 volt supply.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	− 0.5 to +7 Volts ①
Power Dissipation	1 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		$V_{CC} + 0.5$	V	
Output Low Voltage (Ports 4-7)	V_{OL1}			0.45	V	$I_{OL} = 5$ mA ①
Output Low Voltage (Port 7)	V_{OL2}			1	V	$I_{OL} = 20$ mA
Output Low Voltage (Port 2)	V_{OL3}			0.45	V	$I_{OL} = 0.6$ mA
Output High Voltage (Ports 4-7)	V_{OH1}	2.4			V	$I_{OH} = 240\ \mu A$
Output High Voltage (Port 2)	V_{OH2}	2.4			V	$I_{OH} = 100\ \mu A$
Sum of All I_{OL} From 16 Outputs	I_{OL}			100	mA	5 mA Each Pin
Input Leakage Current (Ports 4-7)	I_{IL1}	-10		20	µA	$V_{IN} = V_{CC}$ to 0V
Input Leakage Current (Port 2, $\overline{CS}$, PROG)	I_{IL2}	-10		10	µA	$V_{IN} = V_{CC}$ to 0V
V_{CC} Supply Current	I_{CC}		10	20	mA	

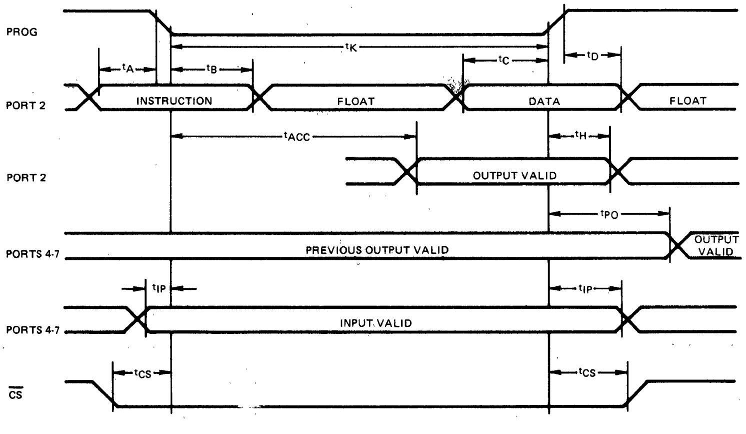
Note: ① Refer to graph of additional sink current drive.

AC CHARACTERISTICS

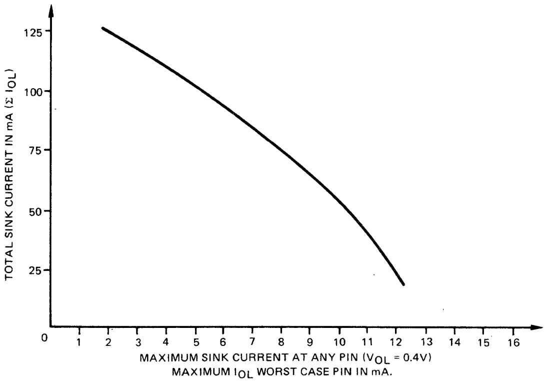
$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Code Valid Before PROG	t_A	100			ns	80 pF Load
Code Valid After PROG	t_B	60			ns	20 pF Load
Data Valid Before PROG	t_C	200			ns	80 pF Load
Data Valid After PROG	t_D	20			ns	20 pF Load
Port 2 Floating After PROG	t_H	0		150	ns	20 pF Load
PROG Negative Pulse Width	t_K	900			ns	
Ports 4-7 Valid After PROG	t_{PO}			700	ns	100 pF Load
Ports 4-7 Valid Before/After PROG	t_{LP1}	100			ns	
Port 2 Valid After PROG	t_{ACC}			750	ns	80 pF Load
$\overline{CS}$ Valid Before/After PROG	$t_{\overline{CS}}$	50			ns	

TIMING WAVEFORMS

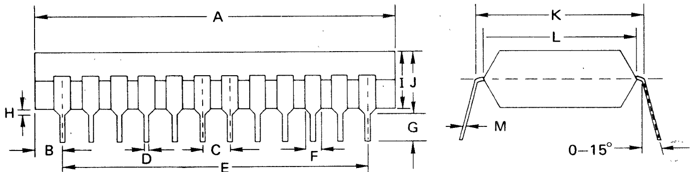


CURRENT SINKING CAPABILITY ①



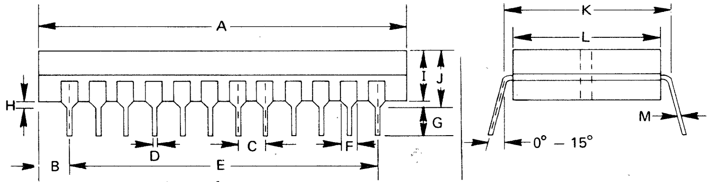
Note: ① This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins. The μPD8243 is capable of sinking 5 mA (for V_{OL} = 0.4V) through each of the 16 I/O lines simultaneously. The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded.

PACKAGE OUTLINES μPD8243C/D



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

NEC Microcomputers, Inc.

NEC
μPD8251
μPD8251A

PROGRAMMABLE COMMUNICATION INTERFACES

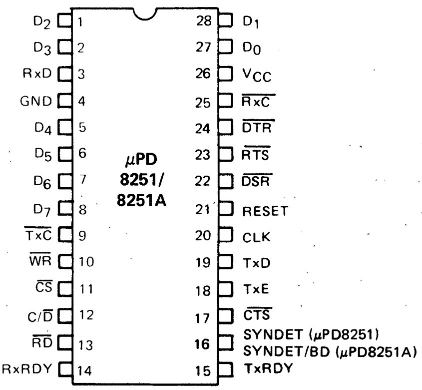
DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters (USARTs) are designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
    - Automatic Break Detect and Handling (μPD8251A)
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate – Synchronous – DC to 56K Baud (μPD8251)
  - – DC to 64K Baud (μPD8251A)
  - – Asynchronous – DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080/8085/μPD780 (Z80™)
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/$\overline{D}$	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock (TTL)
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
SYNDET/BD	Sync Detect/Break Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

TM: Z80 is a registered trademark of Zilog.

Rev/3

FUNCTIONAL DESCRIPTION

The µPD8251 and µPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters are designed specifically for 8080 microcomputer systems but work with most 8-bit processors. Operation of the µPD8251 and µPD8251A, like other I/O devices in the 8080 family, are programmed by system software for maximum flexibility.

In the receive mode, the µPD8251 or µPD8251A converts incoming serial format data into parallel data and makes certain format checks. In the transmit mode, it formats parallel data into serial form. The device also supplies or removes characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

µPD8251A FEATURES AND ENHANCEMENTS

The µPD8251A is an advanced design of the industry standard 8251 USART. It operates with a wide range of microprocessors, including the 8080, 8085, and µPD780 (Z80^{TM}). The additional features and enhancements of the µPD8251A over the µPD8251 are listed below.

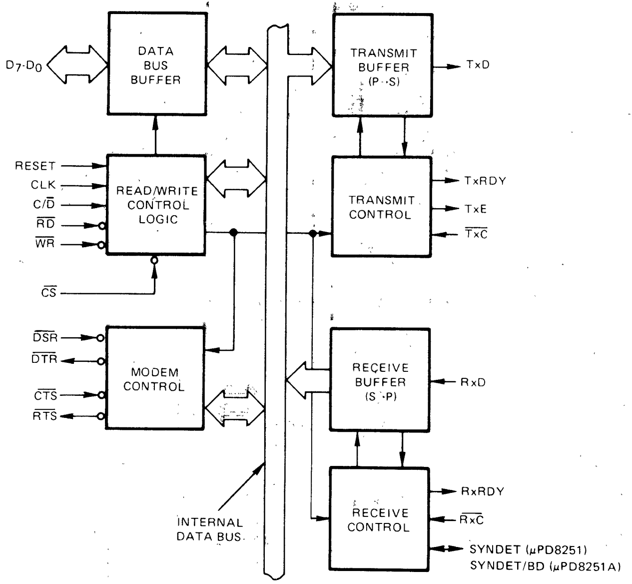
1. The data paths are double-buffered with separate I/O registers for control, status, Data In and Data Out. This feature simplifies control programming and minimizes processor overhead.
2. The Receiver detects and handles "break" automatically in asynchronous operations, which relieves the processor of this task.
3. The Receiver is prevented from starting when in "break" state by a refined Rx initialization. This also prevents a disconnected USART from causing unwanted interrupts.
4. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
5. The Tx Disable command is prevented from halting transmission by the Tx Enable Logic enhancement, until all data previously written has been transmitted. The same logic also prevents the transmitter from turning off in the middle of a word.
6. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through a flip-flop which clears itself upon a status read.
7. The possibility of a false sync detect is minimized by:
   - ensuring that if a double sync character is programmed, the characters be contiguously detected.
   - clearing the Rx register to all Logic 1s (V_{OH}) whenever the Enter Hunt command is issued in Sync mode.
8. The $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device as long as the µPD8251A is not selected.
9. The µPD8251A Status can be read at any time, however, the status update will be inhibited during status read.
10. The µPD8251A has enhanced AC and DC characteristics and is free from extraneous glitches, providing higher speed and improved operating margins.
11. Baud rate from DC to 64K.

BASIC OPERATION

$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	µPD8251/µPD8251A → Data Bus
0	1	0	0	Data Bus → µPD8251/µPD8251A
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

TM:Z80 is a registered trademark of Zilog.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltages	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS					UNIT	TEST CONDITIONS
		μPD8251			μPD8251A			
		MIN	TYP	MAX	MIN	MAX		
Input Low Voltage	V_{IL}	−0.5		0.8	0.5	0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}			0.45		0.45	V	μPD8251: I_{OL} = 1.7 mA μPD8251A: I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			2.4		V	μPD8251: I_{OH} = −100 μA μPD8251A: I_{OH} = −400 μA
Data Bus Leakage	I_{DL}			−50		−10	μA	V_{OUT} = 0.45V
				10		10		V_{OUT} = V_{CC}
Input Load Current	I_{IL}			10		10	μA	At 5.5V
Power Supply Current	I_{CC}		45	80		100	mA	μPD8251A: All Outputs = Logic 1

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V.

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	LIMITS μPD8251 MAX	LIMITS μPD8215A MIN	LIMITS μPD8215A MAX	UNIT	TEST CONDITIONS
READ							
Address Stable before $\overline{READ}$, ($\overline{CS}$, $\overline{C/D}$)	t_{AR}	50		0		ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	430		250		ns	
Data Delay from $\overline{READ}$	t_{RD}		350		200	ns	μPD8251: C_L = 100 pF μPD8251A: C_L = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	25	200	10	100	ns	μPD8251 C_L = 100 pF C_L = 15 pF
WRITE							
Address Stable before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20		0		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		250		ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200		150		ns	
Data Hold Time for WRITE	t_{WD}	40		0		ns	
Recovery Time Between WRITES ②	t_{RV}	6		6		t_{CY}	
OTHER TIMING							
Clock Period ③	t_{CY}	0.420	1.35	0.32	1.35	μs	
Clock Pulse Width High	$t_{\phi W}$	220	$0.7t_{CY}$	120	t_{CY}-90	ns	
Clock Pulse Width Low	$t_{\phi W}$			90		ns	
Clock Rise and Fall Time	t_R, t_F	0	50	5	20	ns	
TxD Delay from Falling Edge of TxC	t_{DTx}		1		1	μs	μPD8251: C_L = 100 pF
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2		2		μs	
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2		2		μs	
Transmitter Input Clock Frequency	f_{Tx}						
1X Baud Rate		DC	56		64	kHz	
16X Baud Rate		DC	520		310	kHz	
64X Baud Rate		DC	520		615	kHz	
Transmitter Input Clock Pulse Width	t_{TPW}						
1X Baud Rate		12		12		t_{CY}	
16X and 64X Baud Rate		1		1		t_{CY}	
Transmitter Input Clock Pulse Delay	t_{TPD}						
1X Baud Rate		15		15		t_{CY}	
16X and 64X Baud Rate		3		3		t_{CY}	
Receiver Input Clock Frequency	f_{Rx}						
1X Baud Rate		DC	56		64	kHz	
16X Baud Rate		DC	520		310	kHz	
64X Baud Rate		DC	520		615	kHz	
Receiver Input Clock Pulse Width	t_{RPW}						
1X Baud Rate		12		12		t_{CY}	
16X and 64X Baud Rate		1		1		t_{CY}	
Receiver Input Clock Pulse Delay	t_{RPD}						
1X Baud Rate		15		15		t_{CY}	
16X and 64X Baud Rate		3		3		t_{CY}	
TxRDY Delay from Center of Data Bit	t_{Tx}		16		8	t_{CY}	μPD8251. C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{RX}		20		24	t_{CY}	
Internal SYNDET Delay from Center of Data Bit	t_{IS}		25		24	t_{CY}	
External SYNDET Set-Up Time before Falling Edge of $\overline{RxC}$	t_{ES}		16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}		16		20	t_{CY}	μPD8251: C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}		16		8	t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}		16		20	t_{CY}	

Notes. ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.

② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

③ The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leqslant 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leqslant 1/(4.5\ t_{CY})$

④ Reset Pulse Width = 6 t_{CY} minimum.

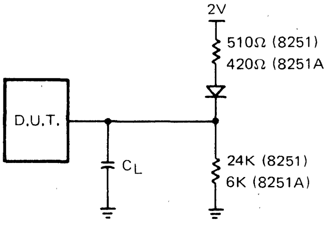
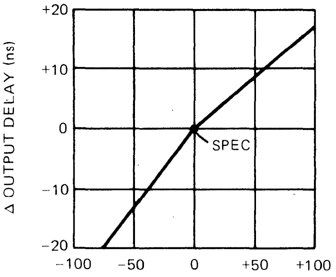


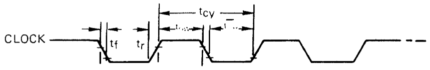
Figure 1.



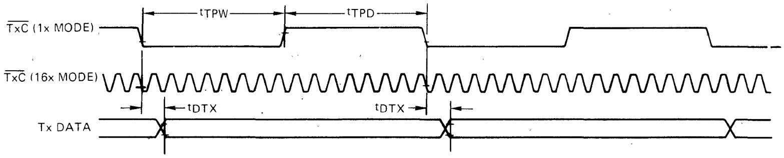
Typical Δ Output Delay Versus Δ Capacitance (pF)

TEST LOAD CIRCUIT

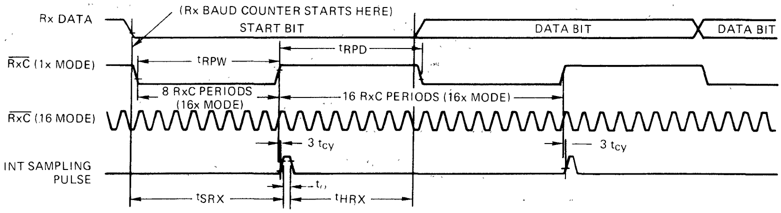
TIMING WAVEFORM



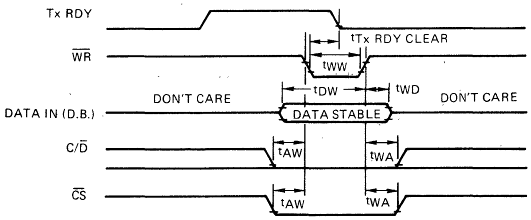
SYSTEM CLOCK INPUT



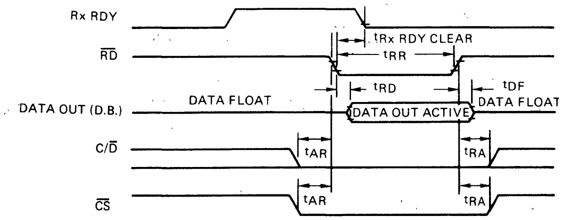
TRANSMITTER CLOCK AND DATA



RECEIVER CLOCK AND DATA



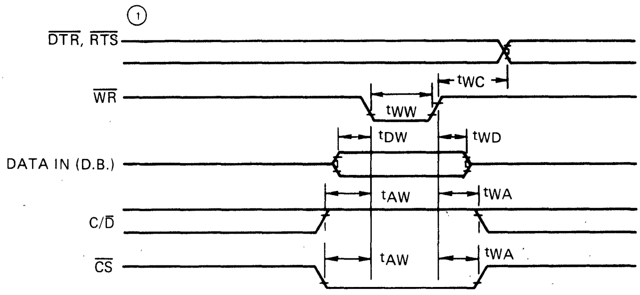
WRITE DATA CYCLE (PROCESSOR → USART)



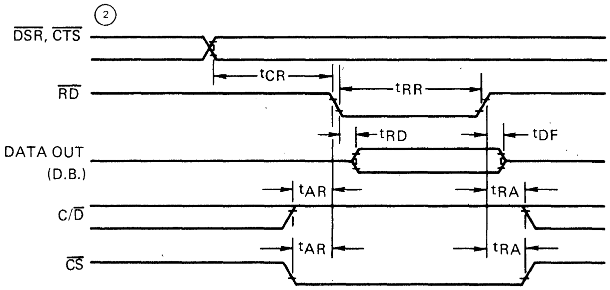
READ DATA CYCLE (PROCESSOR ← USART)

7

TIMING WAVEFORM (CONT.)



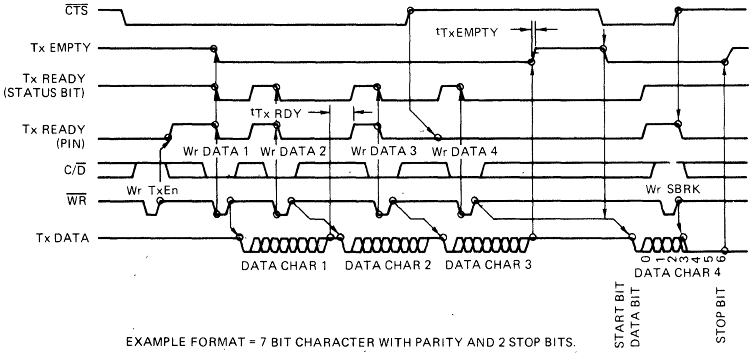
WRITE CONTROL OR OUTPUT PORT CYCLE (PROCESSOR → USART)



READ CONTROL OR INPUT PORT CYCLE (PROCESSOR ← USART)

NOTES: ① T_{WC} Includes the response timing of a control byte.

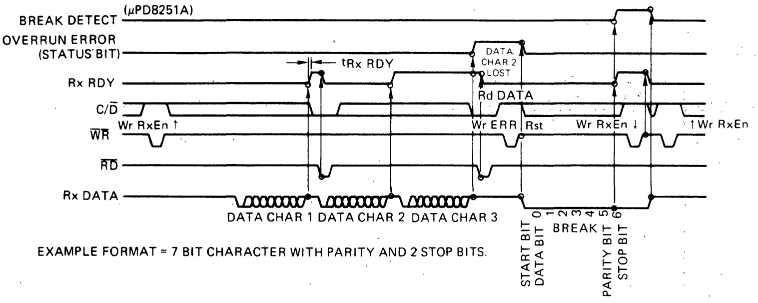
② T_{CR} Includes the effect of CTS on the TxENBL circuitry



EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY AND 2 STOP BITS.

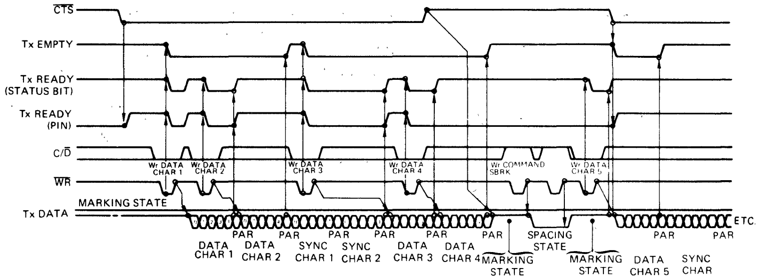
TRANSMITTER CONTROL AND FLAG TIMING (ASYNC MODE)

TIMING WAVEFORM (CONT.)



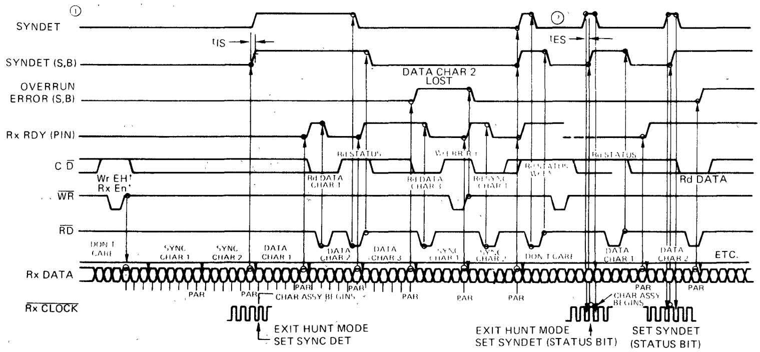
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY AND 2 STOP BITS.

RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



EXAMPLE FORMAT = 5 BIT CHARACTER WITH PARITY AND 2 SYNC CHARACTERS

TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)

Notes: ① Internal sync, 2 sync characters, 5 bits, with parity.
② External sync, 5 bits, with parity.

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the USART to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is 6 t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be at least 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the USART to accept the data or control word which the processor is writing out on the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the USART to place the data or status information onto the Data Bus for the processor to read.
12	$C/\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART to read from or write to the processor.
Modem Control			The μPD8251 and μPD8251A have a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

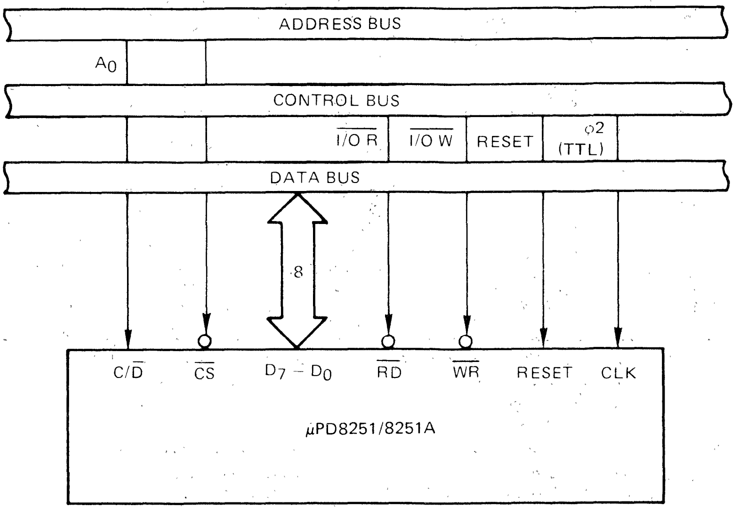
TRANSMIT BUFFER

The Transmit Buffer receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD pin.

PIN IDENTIFICATION (CONT.)

PIN			FUNCTION
NO.	SYMBOL	NAME	
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for polled operation. Loading a character from the processor automatically resets TxRDY, on the leading edge.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{\text{TxC}}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{\text{TxC}}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{\text{TxC}}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{\text{TxC}}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

μPD8251 AND μPD8251A INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVE BUFFER

The Receive Buffer accepts serial data input at the $\overline{\text{RxD}}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 and μPD8251A set the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN			FUNCTION
NO.	SYMBOL	NAME	
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{\text{RxC}}$	Receiver Clock	The Receiver Clock determines the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{\text{RxC}}$ frequency may be 1.16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{\text{RxC}}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{\text{TxC}}$, data is sampled by the μPD8251 and μPD8251A on the rising edge of $\overline{\text{RxC}}$. ①
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET (μPD8251)	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{\text{RxC}}$. The length of the SYNDET input should be at least one $\overline{\text{RxC}}$ period, but may be removed once the μPD8251 is in SYNC.
16	SYNDET/BD (μPD8251A)	Sync Detect/ Break Detect	The SYNDET/BD pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the Break Detect output will go high when an all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx data returns to a logic one state or upon chip reset. The state of Break Detect can be read as a status bit.

Note: ① Since the μPD8251 and μPD8251A will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{\text{RxC}}$ and $\overline{\text{TxC}}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):	If the Baud Rate equals 300:
$\overline{\text{RxC}}$ or $\overline{\text{TxC}}$ equals 110 Hz (1x)	$\overline{\text{RxC}}$ or $\overline{\text{TxC}}$ equals 300 Hz (1x) A or S
$\overline{\text{RxC}}$ or $\overline{\text{TxC}}$ equals 1.76 KHz (16x)	$\overline{\text{RxC}}$ or $\overline{\text{TxC}}$ equals 4800 Hz (16x) A only
$\overline{\text{RxC}}$ or $\overline{\text{TxC}}$ equals 7.04 KHz (64x)	$\overline{\text{RxC}}$ or $\overline{\text{TxC}}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 and μPD8251A to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2) ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 and μPD8251A are ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 and μPD8251A may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 and μPD8251A may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 and μPD8251A cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new control words.

USART PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D} = 1$) followed by a software reset command instruction (40 Hex) can be used to initialize the μPD8251 and μPD8251A.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

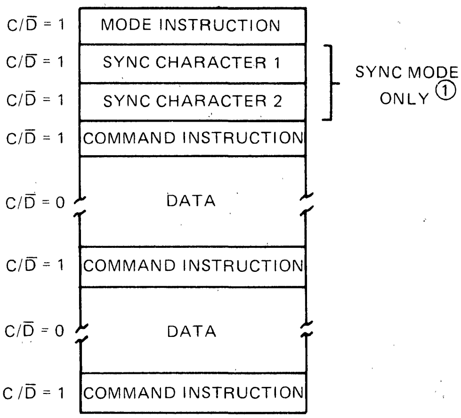
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE ① The second SYNC character is skipped if MODE instruction has programmed the μPD8251 and μPD8251A to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the μPD8251 and μPD8251A to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 and μPD8251A can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

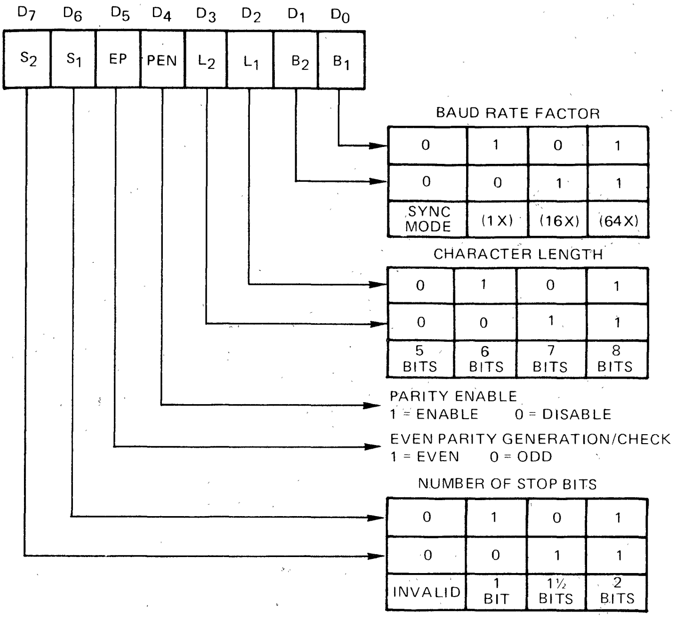
When a data character is written into the μPD8251 and μPD8251A, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{\text{CTS}}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of TxC at TxC, TxC/16 or TxC/64, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251 and μPD8251A, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

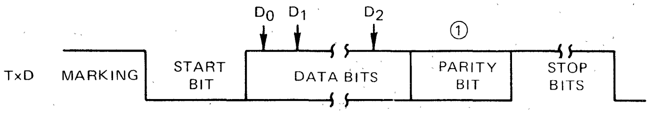
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the date, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{\text{RxC}}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and μPD8251A and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

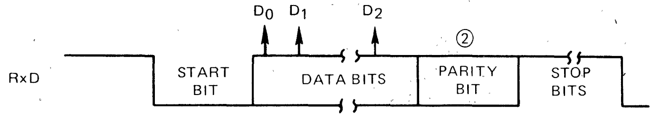
MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE



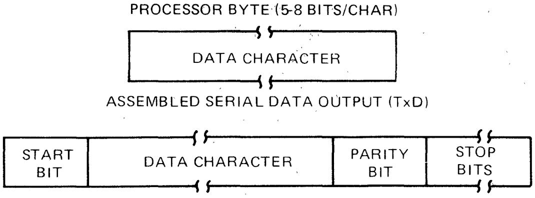
TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



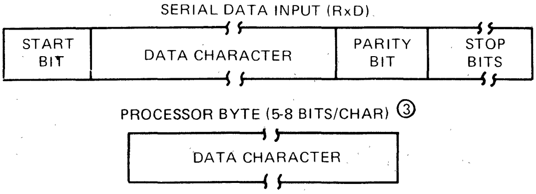
TRANSMITTER OUTPUT



RECEIVER INPUT



TRANSMISSION FORMAT



RECEIVE FORMAT

Notes: ① Generated by μPD8251/8251A
② Does not appear on the Data Bus.
③ If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero."

SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 and μPD8251A receive the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 and μPD8251A Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 and μPD8251A become empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

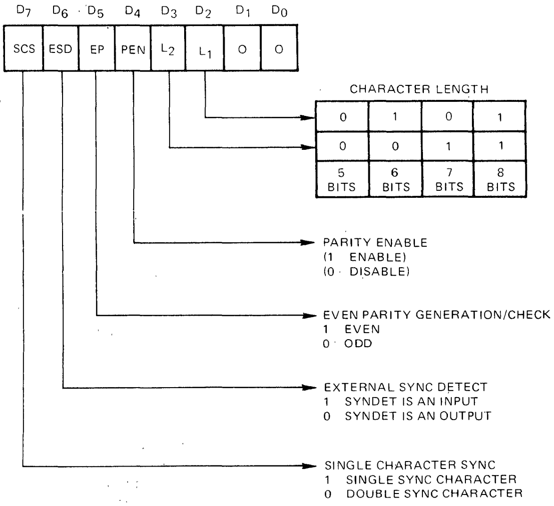
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receive Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 and μPD8251A leave the HUNT mode and are in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

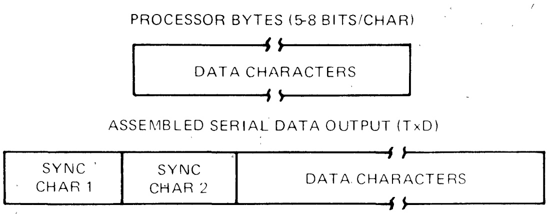
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

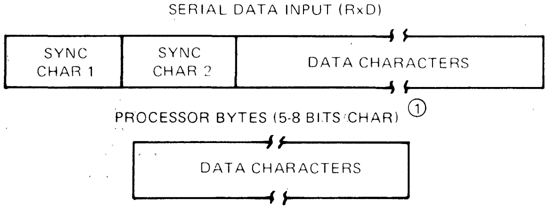
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

Note: ① If character length is defined as 5, 6 or 7 bits, the unused bits are set to "zero."

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 and μPD8251A has been specified by the Mode Instruction and the SYNC character(s) have been entered (if in SYNC mode), the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s) (as needed) are loaded, all subsequent "control writes" ($C/\overline{D}$ = 1) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 and μPD8251A to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the status of an active interface device to determine if errors have occurred or if there are other conditions which require a response from the processor. The μPD8251 and μPD8251A have features which allow the processor to read the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 and μPD8251A to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of 16 clock periods in the μPD8251 and 28 clock periods in the μPD8251A.

PARITY ERROR

When a parity error is detected, the PE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

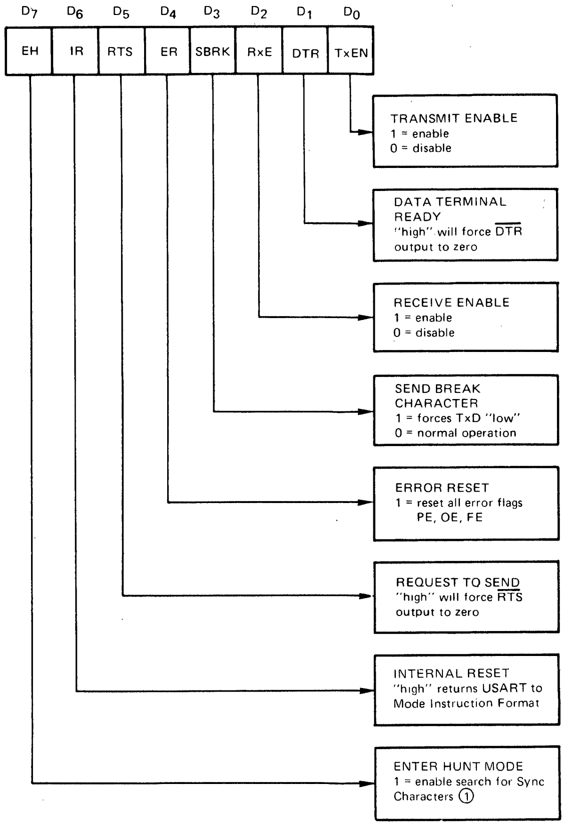
If the processor fails to read a data character before the one following is available, the OE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

If a valid STOP bit is not detected at the end of a character, the FE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

COMMAND INSTRUCTION FORMAT



TRANSMIT ENABLE
1 = enable
0 = disable

DATA TERMINAL READY
"high" will force $\overline{DTR}$ output to zero

RECEIVE ENABLE
1 = enable
0 = disable

SEND BREAK CHARACTER
1 = forces TxD "low"
0 = normal operation

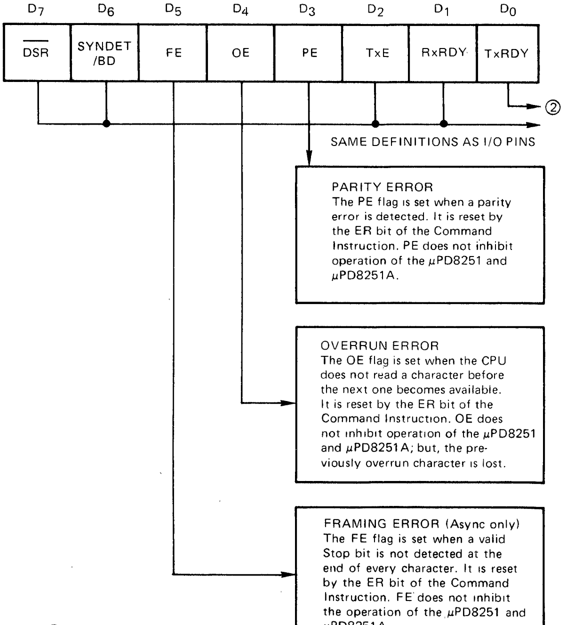
ERROR RESET
1 = reset all error flags PE, OE, FE

REQUEST TO SEND
"high" will force $\overline{RTS}$ output to zero

INTERNAL RESET
"high" returns USART to Mode Instruction Format

ENTER HUNT MODE
1 = enable search for Sync Characters ①

STATUS READ FORMAT



PARITY ERROR
The PE flag is set when a parity error is detected. It is reset by the ER bit of the Command Instruction. PE does not inhibit operation of the μPD8251 and μPD8251A.

OVERRUN ERROR
The OE flag is set when the CPU does not read a character before the next one becomes available. It is reset by the ER bit of the Command Instruction. OE does not inhibit operation of the μPD8251 and μPD8251A; but, the previously overrun character is lost.

FRAMING ERROR (Async only)
The FE flag is set when a valid Stop bit is not detected at the end of every character. It is reset by the ER bit of the Command Instruction. FE does not inhibit the operation of the μPD8251 and μPD8251A.

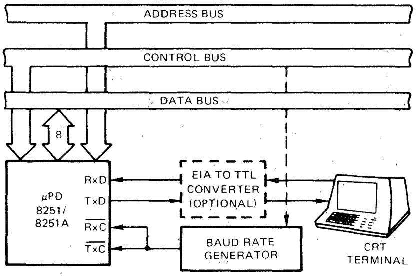
Notes: ① No effect in ASYNC mode.

② TxRDY status bit is not totally equivalent to the $\overline{TxRDY}$ output pin, the relationship is as follows:

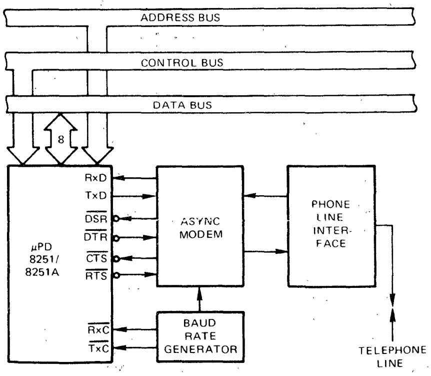
TxRDY status bit = DB Buffer Empty

TxRDY (pin 15) = DB Buffer Empty • $\overline{CTS}$ • TxEn

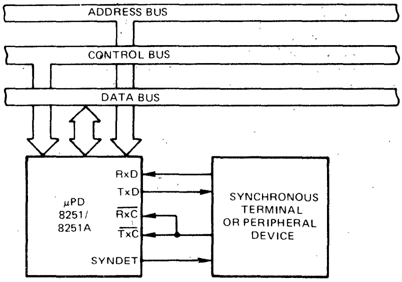
APPLICATION OF THE µPD8251 AND µPD8251A



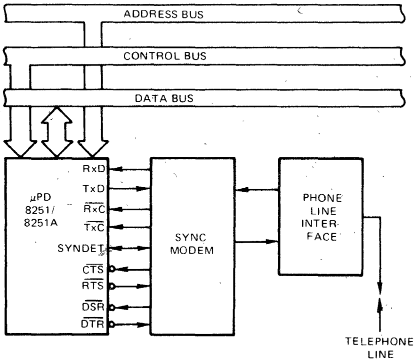
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

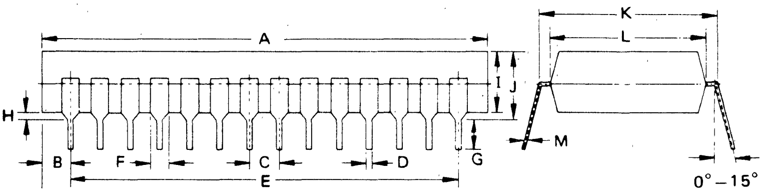


SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



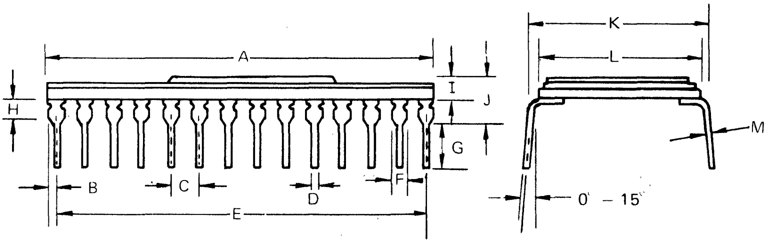
SYNCHRONOUS INTERFACE TO TELEPHONE LINES

PACKAGE OUTLINES
μPD8251C/D
μPD8251AC/D



Plastic

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.41 MAX.
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

NEC

μPD8253
μPD8253-5

PROGRAMMABLE INTERVAL TIMER

DESCRIPTION

The NEC μPD8253 contains three independent, programmable, multi-modal 16-bit counter/timers. It is designed as a general purpose device, fully compatible with the 8080 family. The μPD8253 interfaces directly to the busses of the processor as an array of I/O ports.

The μPD8253 can generate accurate time delays under the control of system software. The three independent 16-bit counters can be clocked at rates from DC to 2 MHz. The system software controls the loading and starting of the counters to provide accurate multiple time delays. The counter output flags the processor at the completion of the time-out cycles.

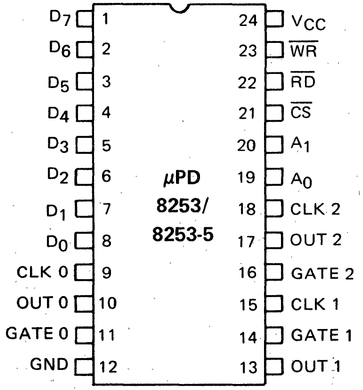
System overhead is greatly improved by relieving the software from the maintenance of timing loops. Some other common uses for the μPD8253 in microprocessor based systems are:

- Programmable Baud Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

FEATURES

- Three Indpendent 16-Bit Counters
- Clock Rate: DC to 3 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5 Volt Supply
- 24 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8-Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0, A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

FUNCTIONAL DESCRIPTION

Data Bus Buffer

The 3-state, 8-bit, bi-directional Data Bus Buffer interfaces the µPD8253 to the 8080A microprocessor system. It will transmit or receive data in accordance with the INput or OUTput instructions executed by the processor. There are three basic functions of the Data Bus Buffer.

1. Program the modes of the µPD8253
2. Load the count registers.
3. Read the count values.

Read/Write Logic

The Read/Write Logic controls the overall operation of the µPD8253 and is governed by inputs received from the processor system bus.

Control Word Register

Two bits from the address bus of the processor, A_0 and A_1, select the Control Word Register when both are at a logic "1" (active-high logic). When selected, the Control Word Register stores data from the Data Bus Buffer in a register. This data is then used to control:

1. The operational MODE of the counters.
2. The selection of BCD or Binary counting.
3. The loading of the count registers.

$\overline{\text{RD}}$ (Read)

This active-low signal instructs the µPD8253 to transmit the selected counter value to the processor.

$\overline{\text{WR}}$ (Write)

This active-low signal instructs the µPD8253 to receive MODE information or counter input data from the processor.

A_1, A_0

The A_1 and A_0 inputs are normally connected to the address bus of the processor. They control the one-of-three counter selection and address the control word register to select one of the six operational MODES.

$\overline{\text{CS}}$ (Chip Select)

The µPD8253 is enabled when an active-low signal is applied to this input. Reading or writing from this device is inhibited when the chip is disabled. The counter operation, however, is not affected.

Counters #0, #1, #2

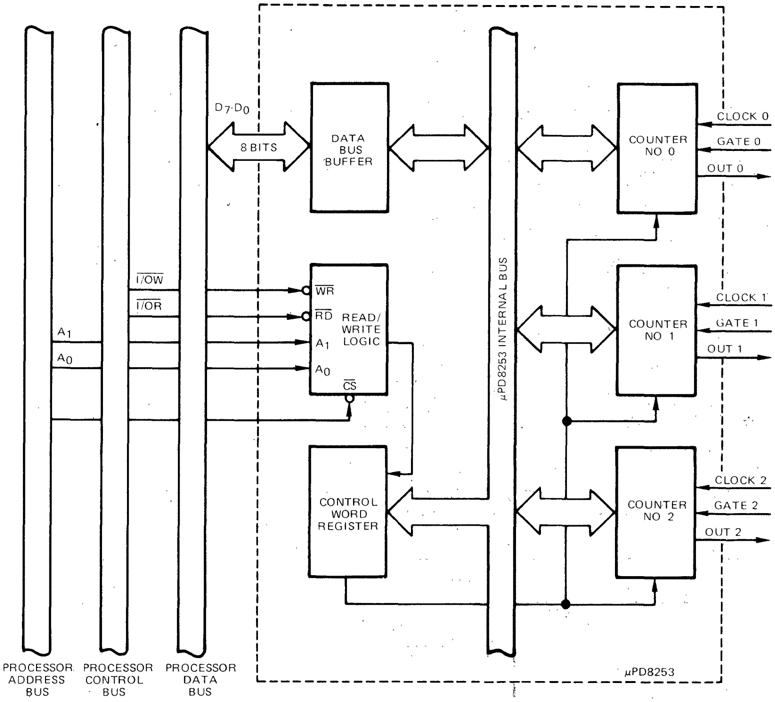
The three identical, 16-bit down counters are functionally independent allowing for separate MODE configuration and counting operation. They function as Binary or BCD counters with their gate, input and output line configuration determined by the operational MODE data stored in the Control Word Register. The system software overhead time can be reduced by allowing the control word to govern the loading of the count data.

The programmer, with READ operations, has access to each counter's contents. The µPD8253 contains the commands and logic to read each counter's contents while still counting without disturbing its operation.

The following is a table showing how the counters are manipulated by the input signals to the Read/Write Logic.

$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	A_1	A_0	FUNCTION
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation, 3-State
1	X	X	X	X	Disable, 3-State
0	1	1	X	X	No-Operation, 3-State

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . 0°C to +70°C
Storage Temperature . . . . −65°C to +125°C
Voltage on Any Pin . . . . −0.5 to +7 Volts①

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device realiability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{IL}			±10	μA	V_{IN} = V_{CC} to 0 V
Output Float Leakage Current	I_{OFL}			±10	μA	V_{OUT} = V_{CC} to 0 V
V_{CC} Supply Current	I_{CC}			95	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Input/Output Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}.

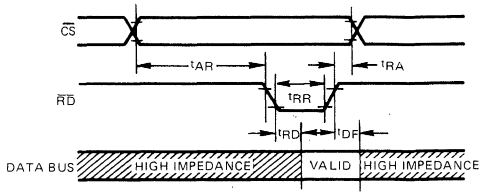
AC CHARACTERISTICS ①

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$; GND = 0V

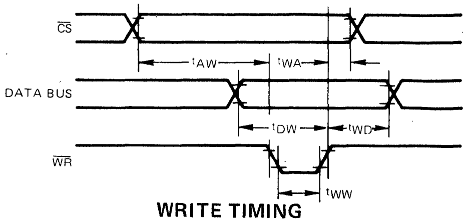
PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD8253			μPD8253-5				
		MIN	TYP	MAX	MIN	TYP	MAX		
READ									
Address Stable Before $\overline{READ}$	t_{AR}	50			50			ns	
Address Hold Time for $\overline{READ}$	t_{RA}	5			5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	400			300			ns	
Data Delay from $\overline{READ}$	t_{RD}			300			200	ns	CL = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}	25		125	25		100	ns	CL = 100 pF
WRITE									
Address Stable Before $\overline{WRITE}$	t_{AW}	20			20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			300			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	200			200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			30			ns	
Recovery Time Between $\overline{WRITES}$	t_{RV}	1			1			μs	
CLOCK AND GATE TIMING									
Clock Period	t_{CLK}	300		DC	300		DC	ns	
High Pulse Width	t_{PWH}	200			200			ns	
Low Pulse Width	t_{PWL}	100			100			ns	
Gate Pulse Width High	t_{GW}	150			150			ns	
Gate Set Up Time to Clock ↑	t_{GS}	100			100			ns	
Gate Hold Time After Clock ↑	t_{GH}	50			50			ns	
Low Gate Width	t_{GL}	100			100			ns	
Output Delay from Clock ↓	t_{OD}			300			300	ns	CL = 100 pF
Output Delay from Gate	t_{ODG}			300			300	ns	CL = 100 pF

Note: ① AC Timing Measured at $V_{OH} = 2.2V$; $V_{OL} = 0.8V$.

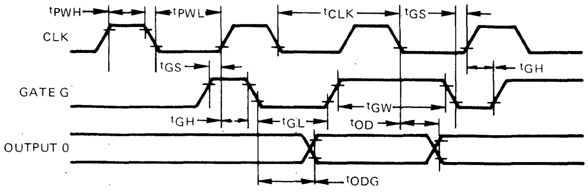
TIMING WAVEFORMS



READ TIMING



WRITE TIMING



CLOCK AND GATE TIMING

PROGRAMMING THE μPD8253

The programmer can select any of the six operational MODES for the counters using system software. Individual counter programming is accomplished by loading the CONTROL WORD REGISTER with the appropriate control word data (A_0, A_1 = 11).

CONTROL WORD FORMAT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC – Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Invalid

RL – Read/Load

RL1	RL0	
0	0	Counter Latching Operation
1	0	Read/Load Most Significant Byte Only
0	1	Read/Load Least Significant Byte Only
1	1	Read/Load Least Significant Byte First, Then Most Significant Byte

BCD

0	Binary Counter, 16-Bits
1	BCD Counter, 4-Decades

M-Mode

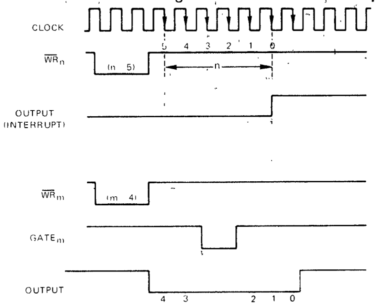
M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

OPERATIONAL MODES ①

Each of the three counters can be individually programmed with different operating MODES by appropriately formatted Control Words. The following is a summary of the MODE operations.

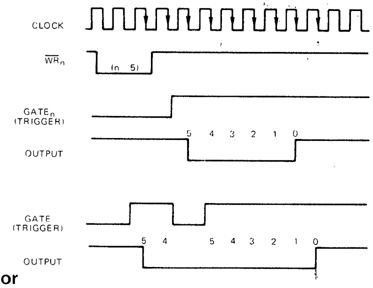
Mode 0: Interrupt on Terminal Count

The initial MODE set operation forces the OUTPUT low. When the specified counter is loaded with the count value, it will begin counting. The OUTPUT will remain low until the terminal count sets it high. It will remain in the high state until the trailing edge of the second $\overline{WR}$ pulse loads in COUNT data. If data is loaded during the counting process, the first $\overline{WR}$ stops the count. Counting starts with the new count data triggered by the falling clock edge after the second $\overline{WR}$. If a GATE pulse is asserted while counting, the count is terminated for the duration of GATE. The falling edge of CLK following the removal of GATE restarts counting from the terminated point.



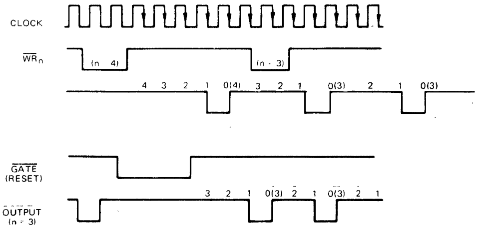
Mode 1: Programmable One-Shot

The OUTPUT is set low by the falling edge of CLOCK following the trailing edge of GATE. The OUTPUT is set high again at the terminal count. The output pulse is not affected if new count data is loaded while the OUTPUT is low. The new data will be loaded on the rising edge of the next trigger pulse. The assertion of a trigger pulse while OUTPUT is low, resets and retriggers the One-Shot. The OUTPUT will remain low for the full count value after the rising edge of TRIGGER.



Mode 2: Rate Generator

The RATE GENERATOR is a variable modulus counter. The OUTPUT goes low for one full CLOCK period as shown in following timing diagram. The count data sets the time between OUTPUT pulses. If the count register is reloaded between output pulses the present period will not be affected. The subsequent period will reflect the new value. The OUTPUT will remain high for the duration of the asserted GATE input. Normal operation resumes on the falling CLOCK edge following the rising edge of GATE.



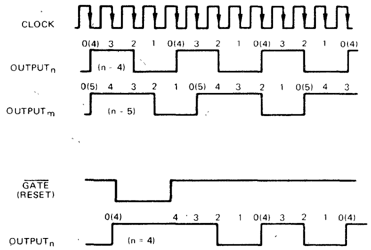
Note: ① All internal counter events occur at the falling edge of the associated clock in all modes of operation.

OPERATIONAL MODES ① (Cont.)

Mode 3: Square Wave Generator

MODE 3 resembles MODE 2 except the OUTPUT will be high for half of the count and low for the other half (for even values of data). For odd values of count data the OUTPUT will be high one clock cycle longer than when it is low (High Period → $\frac{N+1}{2}$ clock cycles; Low Period → $\frac{N-1}{2}$ clock periods, where N is the decimal value of count data). If the count register is reloaded with a new value during counting, the new value will be reflected immediately after the output transition of the current count.

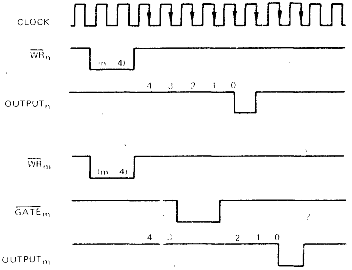
The OUTPUT will be held in the high state while GATE is asserted. Counting will start from the full count data after the GATE has been removed.



Mode 4: Software Triggered Strobe

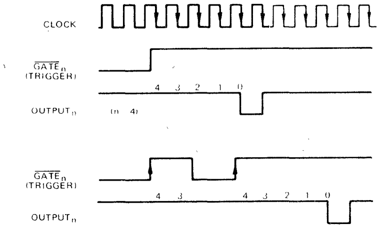
The OUTPUT goes high when MODE 4 is set, and counting begins after the second byte of data has been loaded. When the terminal count is reached, the OUTPUT will pulse low for one clock period. Changes in count data are reflected in the OUTPUT as soon as the new data has been loaded into the count registers. During the loading of new data, the OUTPUT is held high and counting is inhibited.

The OUTPUT is held high for the duration of GATE. The counters are reset and counting begins from the full data value after GATE is removed.

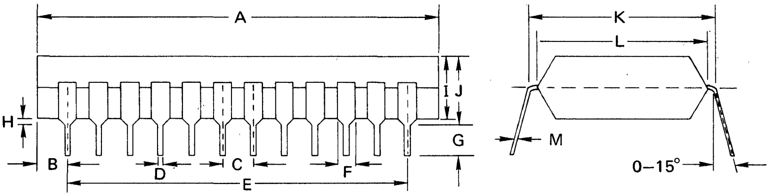


Mode 5: Hardware Triggered Strobe

Loading MODE 5 sets OUTPUT high. Counting begins when count data is loaded and GATE goes high. After terminal count is reached, the OUTPUT will pulse low for one clock period. Subsequent trigger pulses will restart the counting sequence with the OUTPUT pulsing low on terminal count following the last rising edge of the trigger input (Reference bottom half of timing diagram).



PACKAGE OUTLINE
μPD8253C
μPD8253C-5



ITEM	MILLIMETERS	INCHES
A	33 MAX	1 3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25\ ^{+0.10}_{-0.05}$	$0.01\ ^{+0.004}_{-0.0019}$

NEC Microcomputers, Inc.

NEC

µPD8255
µPD8255A-5*

PROGRAMMABLE PERIPHERAL INTERFACES

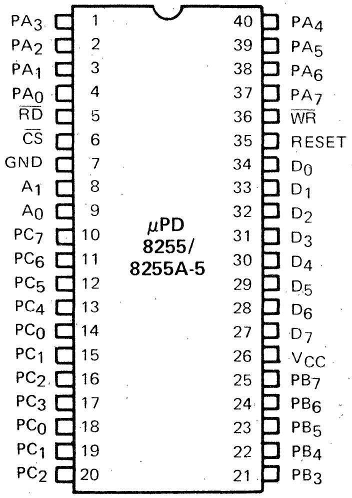
DESCRIPTION

The µPD8255 and µPD8255A-5 are general purpose programmable INPUT/OUTPUT devices designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The µPD8255 and µPD8255A-5 are packaged in 40 pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays (µPD8255)
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays (µPD8255A-5)
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

*All data pertaining to the µPD8255A-5 is preliminary.

Rev/2

General

The μPD8255 and μPD8255A-5 Programmable Peripheral Interfaces (PPI) are designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255 and μPD8255A-5. The μPD8255 and μPD8255A-5 are functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 and μPD8255A-5 can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9
Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255 and μPD8255A-5. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)
Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written <u>into</u>, the contents cannot be read back to the processor.

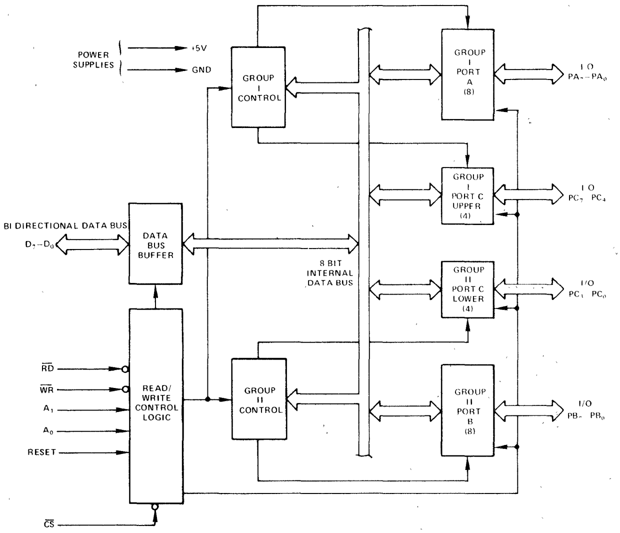
Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255 and μPD8255A-5 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 and μPD8255A-5 is further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$^*T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS µPD8255 MIN			LIMITS µPD8255A-5 MIN			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
Input Low Voltage	V_{IL}	V_{SS}-0.5		0.8	-0.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4			0.45	V	②
Output High Voltage	V_{OH}	2.4			2.4			V	③
Darlington Drive Current	I_{OH} ①	1	2	4	-1	-2	-4	mA	$V_{OH} = 1.5V$, $R_{EXT} = 750\Omega$
Power Supply Current	I_{CC}		40	120		40	120	mA	$V_{CC} = +5V$, Output Open
Input Leakage Current	I_{LIH}			10			10	µA	$V_{IN} = V_{CC}$
Input Leakage Current	I_{LIL}			-10			-10	µA	$V_{IN} = 0.4V$
Output Leakage Current	I_{LOH}			10			10	µA	$V_{OUT} = V_{CC}$, $\overline{CS} = 2.0V$
Output Leakage Current	I_{LOL}			-10			-10	µA	$V_{OUT} = 0.4V$, $\overline{CS} = 2.0V$

Notes. ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5V for µPD8255, or 4 mA into 1.5V for µPD8255A-5.

② For µPD8255 $I_{OL} = 1.7$ mA
For µPD8255A-5, $I_{OL} = 2.5$ mA for DB Port, 1.7 mA for Peripheral Ports

③ For µPD8255 $I_{OH} = -100$ µs for DB Port, 50 µs for Peripheral Ports
For µPD8255A-5 $I_{OH} = -400$ µs for DB Port, −200 µs for Peripheral Ports

CAPACITANCE

$T_a = 25°C$; $V_{CC} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	$f_c = 1$ MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

μPD8255/8255A-5

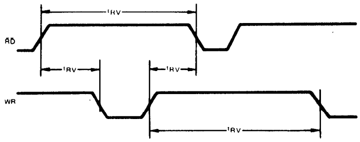
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

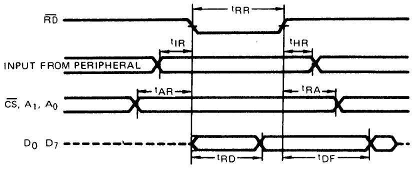
PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		μPD8255		μPD8255A-5			
		MIN	MAX	MIN	MAX		
READ							
Address Stable Before $\overline{READ}$	t_{AR}	50		0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	405		300		ns	
Data Valid From $\overline{READ}$	t_{RD}		295		200	ns	8255: $C_L = 100$ pF 8255A-5: $C_L = 150$ pF
Data Float After $\overline{READ}$	t_{DF}	 10	150	 10	100	ns ns	$C_L = 100$ pF $C_L = 15$ pF
Time Between $\overline{READS}$ and/or $\overline{WRITES}$	t_{RV}	850		850		ns	②
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		300		ns	
Data Valid To $\overline{WRITE}$ (L.E.)	t_{DW}	10		100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	35		30		ns	
OTHER TIMING							
$\overline{WR}$ = 0 To Output	t_{WB}		500		350	ns	8255: $C_L = 50$ pF 8255A-5: $C_L = 150$ pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	50		0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	500		300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		500		ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	60		0		ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150		180		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		400		300	ns	8255: $C_L = 50$ pF 8255A-5: $C_L = 150$ pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}	 20	300	 20	250	ns	8255 $\begin{cases} C_L = 50 \text{ pF} \\ C_L = 15 \text{ pF} \end{cases}$
$\overline{WR}$ = 1 To $\overline{OBF}$ = 0	t_{WOB}		300		650	ns	8255: $C_L = 50$ pF 8255A-5: $C_L = 150$ pF
$\overline{ACK}$ = 0 To $\overline{OBF}$ = 1	t_{AOB}		450		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		450		300	ns	
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		360		300	ns	
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		450		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		400		300	ns	
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		400		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		850		850	ns	

Notes: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

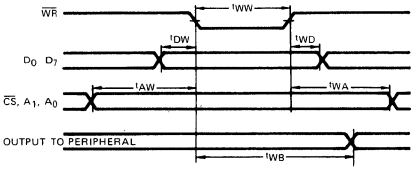
②



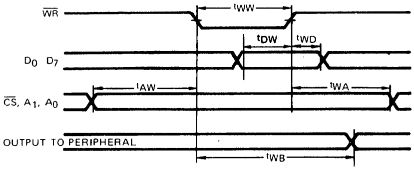
TIMING WAVEFORMS
MODE 0



BASIC INPUT



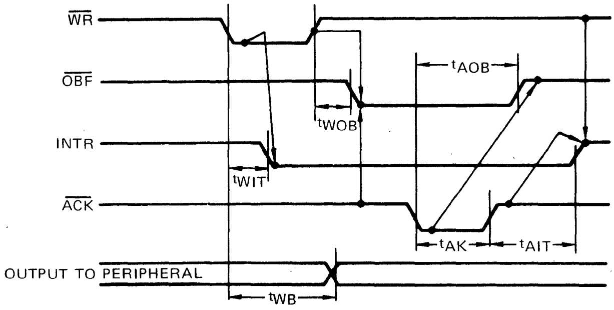
BASIC OUTPUT – μPD8255

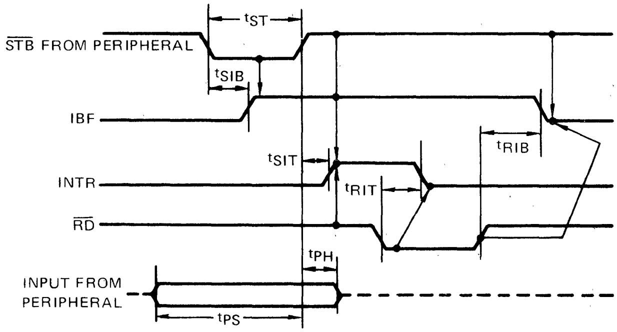


BASIC OUTPUT – μPD8255A-5

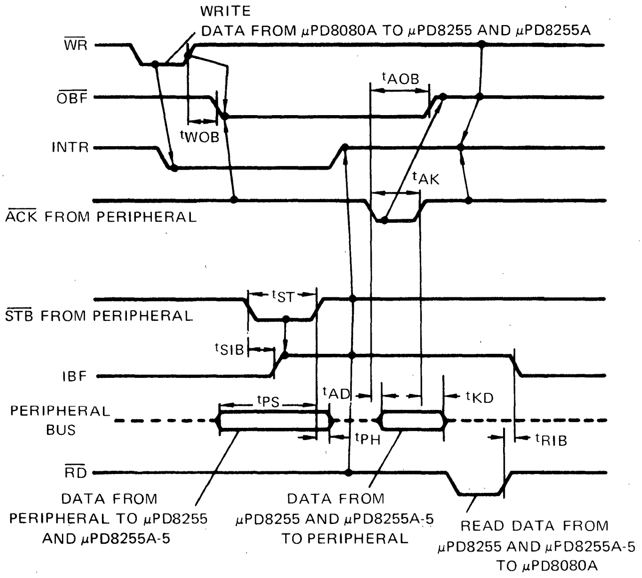
TIMING WAVEFORMS (CONT.)

MODE 1





MODE 2



Note: ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
$(INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR})$

② When the μPD8255A-5 is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

MODES

The μPD8255 and μPD8255A-5 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

  16 different configurations in MODE 0

  Two 8-bit ports and two 4-bit ports

  Inputs are not latched

  Outputs are latched

MODE 1

MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.

Two I/O Groups (I and II)

Both groups contain an 8-bit data port and a 4-bit control/data port

Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.

An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})

Both inputs and outputs are latched

An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

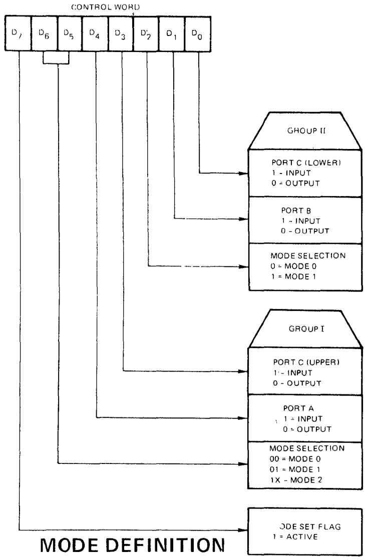
OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

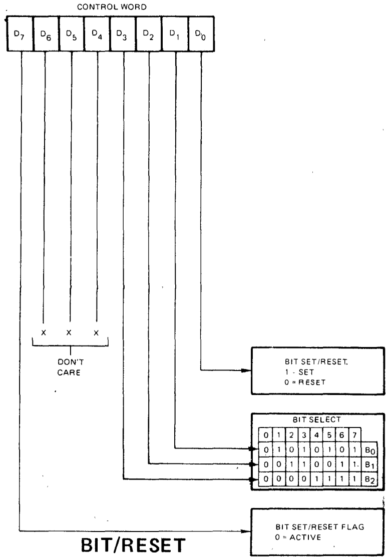
NOTES: ① X means "DO NOT CARE."

② All conditions not listed are illegal and should be avoided.

FORMATS



MODE DEFINITION

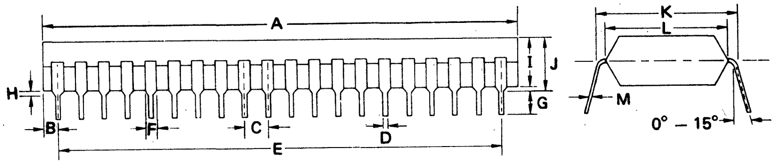


BIT SELECT								
0	1	2	3	4	5	6	7	
0	1	0	1	0	1	0	1	B_0
0	0	1	1	0	0	1	1	B_1
0	0	0	0	1	1	1	1	B_2

BIT/RESET

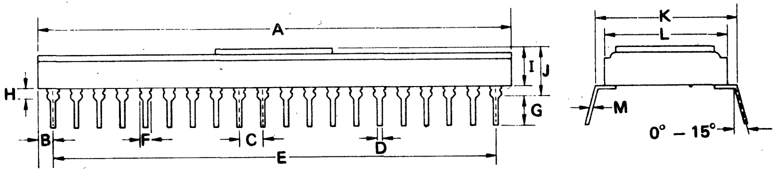
PACKAGE OUTLINE µPD8255C/D µPD8255AC/D-5

Members of the µPD8085 Family are housed in both plastic and ceramic 40 pin packages. The drawings and tables below apply to all five of the NEC Microcomputer parts covered in this data sheet.



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

NEC Microcomputers, Inc.

NEC
µPD8257
µPD8257-5

PROGRAMMABLE DMA CONTROLLER

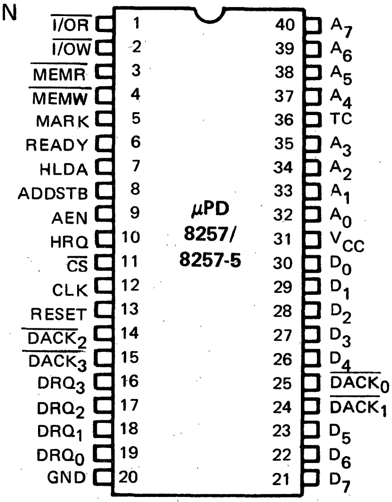
DESCRIPTION

The µPD8257 is a programmable four-channel Direct Memory Access (DMA) controller It is designed to simplify high speed transfers between peripheral devices and memories. Upon a peripheral request, the 8257 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the 8257 so that the system bus may be acquired by the generation of a single HOLD command to the 8080. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other 8257 devices for systems requiring more than four DMA channels.

FEATURES

- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Automatic Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- 40 Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus
A_7-A_0	Address Bus
$\overline{\text{I/OR}}$	I/O Read
$\overline{\text{I/OW}}$	I/O Write
$\overline{\text{MEMR}}$	Memory Read
$\overline{\text{MEMW}}$	Memory Write
CLK	Clock Input
RESET	Reset Input
READY	Ready
HRQ	Hold Request (to 8080A)
HLDA	Hold Acknowledge (from 8080A)
AEN	Address Enable
ADSTB	Address Strobe
TC	Terminal Count
MARK	Modulo 128 Mark
DRQ_3-DRQ_0	DMA Request Input
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA Acknowledge Out
$\overline{\text{CS}}$	Chip Select
V_{CC}	+5 Volts
GND	Ground

FUNCTIONAL DESCRIPTION

The 8257 is a programmable, Direct Memory Access (DMA) device and when used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080 based systems. Once initialized by an 8080 CPU, the 8257 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU, and it will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occur within the 8257.

- It acquires control of the system bus (placing 8080 in hold mode).
- Resolves priority conflicts if multiple DMA requests are made.
- A 16 bit memory address word is generated with the aid of an 8212 in the following manner:

  The 8257 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.

  The 8257 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.
- The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

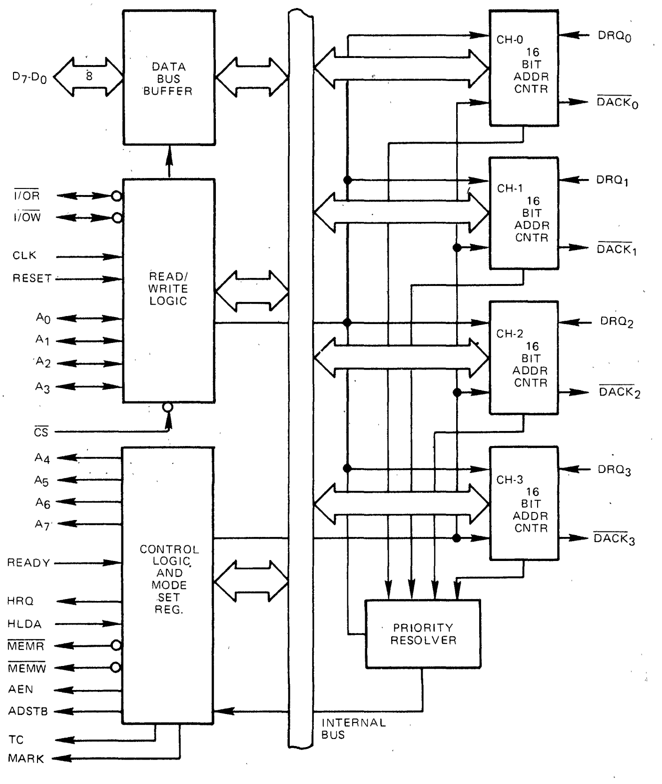
Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA Request (DRQ_n). The 8257 retains control of the system bus as long as DRQ_n remains high or until the Terminal Count (TC) is reached. When the Terminal Count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

- DMA read; which causes data to be transferred from memory to a peripheral;
- DMA write; which causes data to be transferred from a peripheral to memory; and
- DMA verify; which does not actually involve the transfer of data.

The DMA read and write modes are the normal operating conditions for the 8257. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA Acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (Cyclic Redundancy Code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

BLOCK DIAGRAM



AC CHARACTERISTICS PERIPHERAL (SLAVE) MODE

BUS PARAMETERS

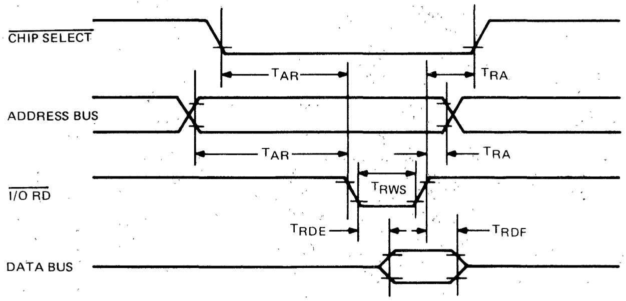
T_a = 0°C to 70°C; V_{CC} = 5V ± 5%; GND = 0V ①

PARAMETER	SYMBOL	LIMITS µPD8257 MIN	TYP	MAX	µPD8257-5 MIN	TYP	MAX	UNIT	TEST CONDITIONS
READ									
Adr or $\overline{CS}$↓ Setup to $\overline{Rd}$↓	T_{AR}	0			0			ns	
Adr or $\overline{CS}$↑ Hold from $\overline{Rd}$↑	T_{RA}	0			0			ns	
Data Access from $\overline{Rd}$↓	T_{RDE}	0		300	0		200	ns	C_L = 100 pF
DB→Float Delay from $\overline{Rd}$↑	T_{RDF}	20		150	20		150	ns ns	C_L = 100 pF C_L = 15 pF
$\overline{Rd}$ Width	T_{RW}	250			250			ns	
WRITE									
$\overline{CS}$↓ Setup to $\overline{Wr}$↓	T_{CW}	300			300			ns	
$\overline{CS}$↑ Hold from $\overline{Wr}$↑	T_{WC}	20			20			ns	
Adr Setup to $\overline{Wr}$↓	T_{AW}	20			20			ns	
Adr Hold from $\overline{Wr}$↑	T_{WA}	0			0			ns	
Data Setup to $\overline{Wr}$↓	T_{DW}	200			200			ns	
Data Hold from $\overline{Wr}$↑	T_{WD}	0			0			ns	
Wr Width	T_{WWS}	200			200			ns	
OTHER TIMING									
Reset Pulse Width	T_{RSTW}	300			300			ns	
Power Supply ↑(V_{CC}) Setup to Reset↓	T_{RSTD}	500			500			µs	
Signal Rise Time	T_r			20			20	ns	
Signal Fall Time	T_f			20			20	ns	
Reset to First $\overline{IOWR}$	T_{RSTS}	2			2			t_{CY}	

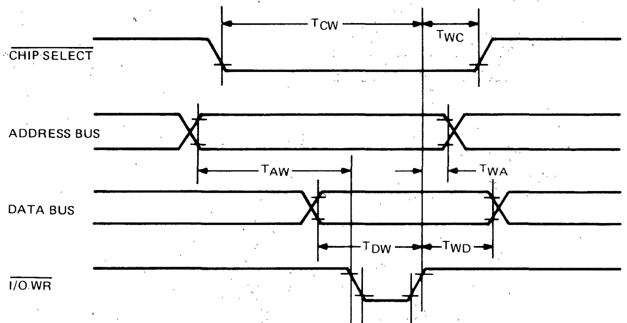
Note: ① All timing measurements are made at the following reference voltages unless specified otherwise Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.

TIMING WAVEFORMS PERIPHERAL (SLAVE) MODE

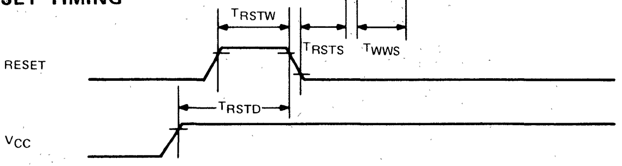
READ TIMING



WRITE TIMING



RESET TIMING



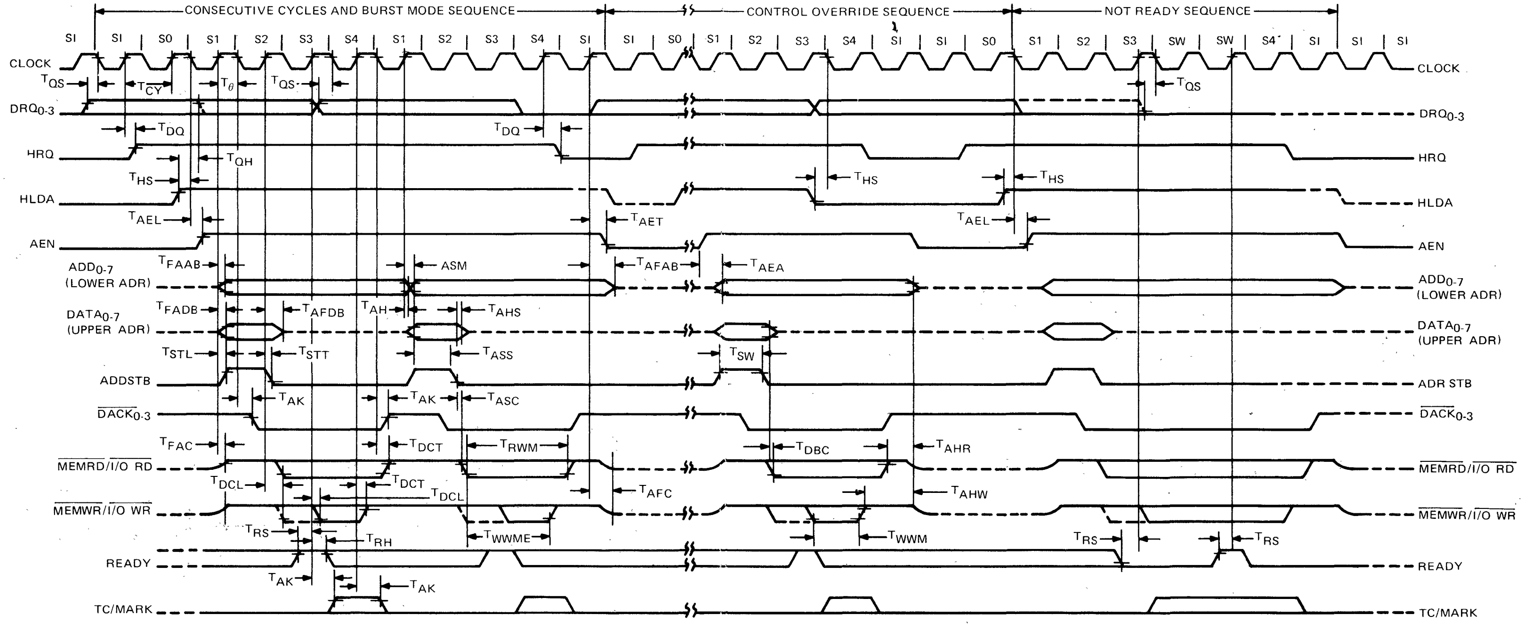
AC CHARACTERISTICS DMA (MASTER) MODE

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$; GND = 0V

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		μPD8257		μPD8257-5			
		MIN	MAX	MIN	MAX		
Cycle Time (Period)	T_{CY}	0.320	4	0.320	4	μs	
Clock Active (High)	T_{θ}	120	$.8T_{CY}$	80	$.8T_{CY}$	ns	
DRQ↑ Setup to θ↓ (SI, S4)	T_{QS}	120		120			
DRQ↓ Hold from HLDA↑	T_{QH}	0		0			④
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 2.0V)	T_{DQ}		160		160	ns	①
HRQ↑ or ↓ Delay from θ↑ (SI, S4) (measured at 3.3V)	T_{DQ1}		250		250	ns	③
HLDA↑ or ↓Setup to θ↓ (SI, S4)	T_{HS}	100		100		ns	
AEN↑ Delay from θ↓ (S1)	T_{AEL}		300		300	ns	①
AEN↓ Delay from θ↑ (SI)	T_{AET}		200		200	ns	①
Adr (AB) (Active) Delay from AEN↑ (S1)	T_{AEA}	20		20		ns	④
Adr (AB) (Active) Delay from θ↑ (S1)	T_{FAAB}		250		250	ns	②
Adr (AB) (Float) Delay from θ↑ (SI)	T_{AFAB}		150		150	ns	②
Adr (AB) (Stable) Delay from θ↑ (S1)	T_{ASM}		250		250	ns	②
Adr (AB) (Stable) Hold from θ↑ (S1)	T_{AH}	$T_{ASM}-50$		$T_{ASM}-50$			②
Adr (AB) (Valid) Hold from $\overline{Rd}$↑ (S1, SI)	T_{AHR}	60		60		ns	④
Adr (AB) (Valid) Hold from $\overline{Wr}$↑ (S1, SI)	T_{AHW}	300		300		ns	④
Adr (DB) (Active) Delay from θ↑ (S1)	T_{FADB}		300		300	ns	②
Adr (DB) (Float) Delay from θ↑ (S2)	T_{AFDB}	$T_{STT}+20$	250	$T_{STT}+20$	170	ns	②
Adr (DB) Setup to Adr Stb↓ (S1-S2)	T_{ASS}	100		100		ns	④
Adr (DB) (Valid) Hold from Adr Stb↓ (S2)	T_{AHS}	50		50		ns	④
Adr Stb↑ Delay from θ↑ (S1)	T_{STL}		200		200	ns	①
Adr Stb↓ Delay from θ↑ (S2)	T_{STT}		140		140	ns	①
Adr Stb Width (S1-S2)	T_{SW}	$T_{CY}-100$		$T_{CY}-100$		ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr Stb↓ (S2)	T_{ASC}	70		70		ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr (DB) (Float) (S2)	T_{DBC}	20		20		ns	④
DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark ↑ Delay from θ↑ (S3) and TC/Mark ↓ Delay from θ↑ (S4)	T_{AK}		250		250	ns	① ⑤
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{Wr}$↓ Delay from θ↑ (S3)	T_{DCL}		200		200	ns	② ⑥
$\overline{Rd}$↑ Delay from θ↓ (S1, SI) and $\overline{Wr}$↑ Delay from θ↑ (S4)	T_{DCT}		200		200	ns	② ⑦
$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑ (S1)	T_{FAC}		300		300	ns	②
$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑ (SI)	T_{AFC}		150		150	ns	②
$\overline{Rd}$ Width (S2-S1 or SI)	T_{RWM}	$2T_{CY}+T_{\theta}-50$		$2T_{CY}+T_{\theta}-50$		ns	④
$\overline{Wr}$ Width (S3-S4)	T_{WWM}	$T_{CY}-50$		$T_{CY}-50$		ns	④
$\overline{Wr}$ (Ext) Width (S2-S4)	T_{WWME}	$2T_{CY}-50$		$2T_{CY}-50$		ns	④
READY Set Up Time to θ↑ (S3, Sw)	T_{RS}	30		30		ns	
READY Hold Time from θ↑ (S3, Sw)	T_{RH}	20		20		ns	

Notes: ① Load = 1 TTL
② Load = 1 TTL + 50 pF
③ Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V
④ Tracking Specification
⑤ $\Delta T_{AK} < 50$ ns
⑥ $\Delta T_{DGL} < 50$ ns
⑦ $\Delta T_{DCT} < 50$ ns

TIMING WAVEFORMS
DMA (MASTER) MODE



DMA OPERATION

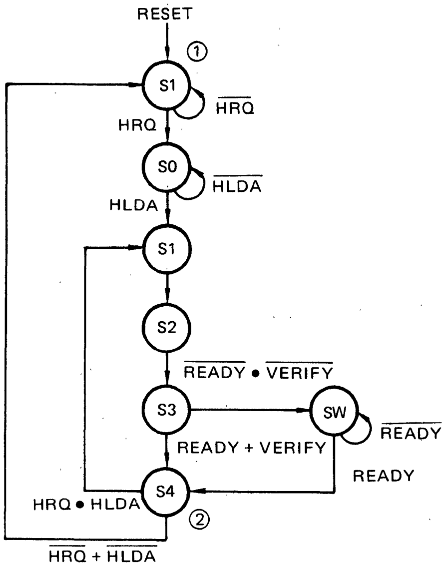
Internally the 8257 contains six different states (S0, S1, S2, S3, S4 and SW), the duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA Requests (DRQ_n), then the 8257 enters the S0 state. During state S0 a Hold Request (HRQ) is sent to the 8080 and the 8257 waits in S0 until the 8080 issues a Hold Acknowledge (HLDA) back. During S0, DMA Requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme). After receipt of HLDA, the DMA Acknowledge line ($\overline{DACK_n}$) with the highest priority is driven low selecting that particular peripheral for the DMA cycle. The DMA Request line (DRQ_n) must remain high until either a DMA Acknowledge ($\overline{DACK_n}$) or both $\overline{DACK_n}$ and TC (Terminal Count) occur, indicating the end of a block or sector transfer (burst mode).

The DMA cycle consists of four internal states; S1, S2, S3 and S4. If the access time of the memory or I/O device is not fast enough to return a Ready command to the 8257 after it reaches state S3, then a Wait state is initiated (SW). One or more than one Wait state occurs until a Ready signal is received, and the 8257 is allowed to go into state S4. Either the extended write option or the DMA Verify mode may eliminate any Wait state.

If the 8257 should lose control of the system bus (i.e., HLDA goes low) then the current DMA cycle is completed, the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the 8257 and the 8080.

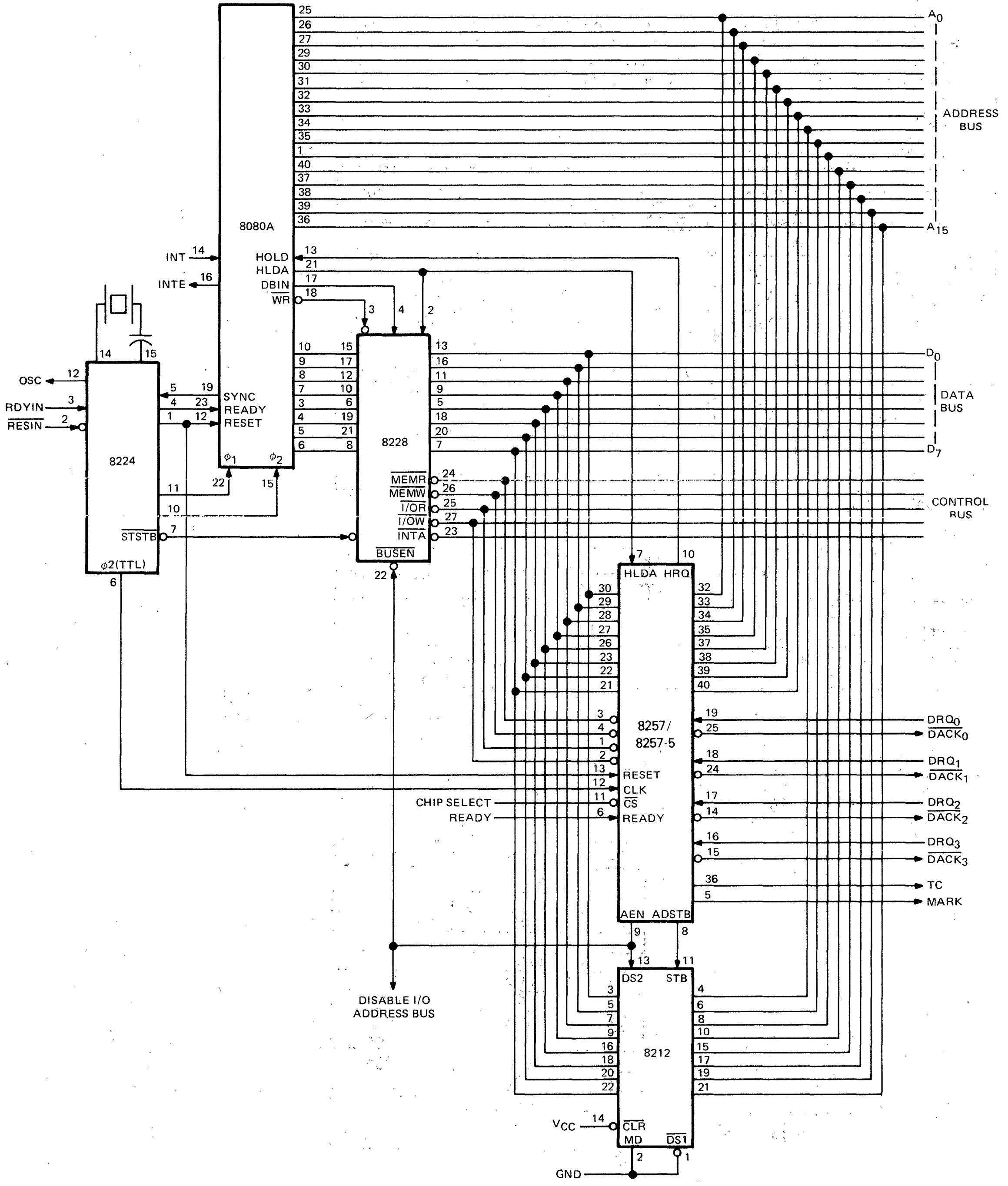
During DMA write cycles, the I/O Read ($\overline{I/O\ R}$) output is generated at the beginning of state S2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S2 and the I/O Write ($\overline{I/O\ W}$) goes low at the beginning of state S3. No Read or Write control signals are generated during DMA verify cycles.

DMA OPERATION STATE DIAGRAM



Notes: ① HRQ is set if DRQ_n is active.
② HRQ is reset if DRQ_n is not active.

TYPICAL 8257 SYSTEM INTERFACE SCHEMATIC



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . 0°C to +70°C

Storage Temperature . . . . –65°C to +150°C

Voltage on Any Pin . . . . –0.5 to +7 Volts ①

Power Dissipation . . . . 1 Watt

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$; GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Low Voltage	V_{IL}	–0.5		0.8	Volts	
Input High Voltage	V_{IH}	2.0		$V_{CC} + 0.5$	Volts	
Output Low Voltage	V_{OL}			0.45	Volts	$I_{OL} = 1.6$ mA
Output High Voltage	V_{OH}	2.4		V_{CC}	Volts	$I_{OH} = -150$ μA for AB, DB and AEN $I_{OH} = -80$ μA for others
HRQ Output High Voltage	V_{HH}	3.3		V_{CC}	Volts	$I_{OH} = -80$ μA
V_{CC} Current Drain	I_{CC}			120	mA	
Input Leakage	I_{IL}			10	μA	$V_{IN} = V_{CC}$
Output Leakage During Float	I_{OFL}			10	μA	V_{OUT}①

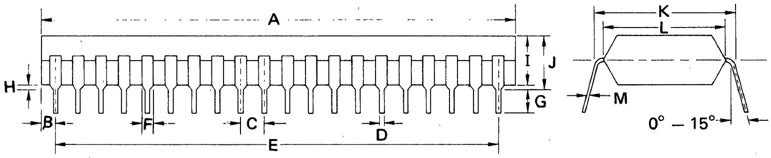
Note: ① $V_{CC} > V_{OUT} > GND + 0.45V$

CAPACITANCE

$T_a = 25°C$; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			10	pF	$f_c = 1$ MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE
μPD8257C
μPD8257C-5



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

NEC

NEC Microcomputers, Inc.

μPD8259
μPD8259-5*

PROGRAMMABLE INTERRUPT CONTROLLER

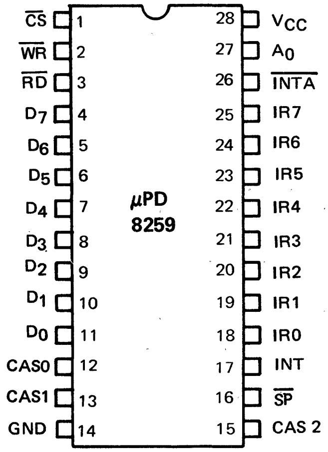
DESCRIPTION

The NEC μPD8259 is a programmable interrupt controller directly compatible with the 8080A/8085A/μPD780(Z80™). It can service eight levels of interrupts and contains on-chip logic to expand interrupt capabilities up to sixty-four levels with the addition of other μPD8259's. The user is offered a selection of priority algorithms to tailor the priority processing to meet his systems requirements. These algorithms can be dynamically modified during operation, expanding the versatility of the microprocessor system.

FEATURES

- Eight Level Priority Controller
- Programmable Base Vector Address
- Expandable to 64 Levels
- Programmable Interrupt Modes (Algorithms)
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Full Compatibility with 8080A/μPD780(Z80™)
- μPD8259-5 Compatible with 8085A Speeds
- Available in 28 Pin Plastic and Ceramic Packages

PIN CONFIGURATION



PIN NAMES

$D_7 - D_0$	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
CAS2 – CAS0	Cascade Lines
$\overline{SP}$	Slave Program Input
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 – IR7	Interrupt Request Inputs
$\overline{CS}$	Chip Select

*All data pertaining to the μPD8259-5 is preliminary.

TM: Z80 is a registered trademark of Zilog, Inc.

BASIC FUNCTIONAL DESCRIPTION

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupt request register and in-service register store the in-coming interrupt request signals appearing on the IR0-7 lines (refer to functional block diagram). The inputs requesting service are stored in the IRR while the interrupts actually being serviced are stored in the ISR.

A positive transition on an IR input sets the corresponding bit in the Interrupt Request Register, and at the same time the INT output of the μPD8259 is set high. The IR input line must remain high until the first $\overline{\text{INTA}}$ input has been received. Multiple, non-masked interrupts occurring simultaneously can be stored in the IRR. The incoming $\overline{\text{INTA}}$ sets the appropriate ISR bit (determined by the programmed interrupt algorithm) and resets the corresponding IRR bit. The ISR bit stays high-active during the interrupt service subroutine until it is reset by the programmed End-of-Interrupt (EOI) command.

PRIORITY RESOLVER

The priority resolver decides the priority of the interrupt levels in the IRR. When the highest priority interrupt is determined it is loaded into the appropriate bit of the In-Service register by the first $\overline{\text{INTA}}$ pulse.

DATA BUS BUFFER

The 3-state, 8-bit, bi-directional data bus buffer interfaces the μPD8259 to the processor's system bus. It buffers the Control Word and Status Data transfers between the μPD8259 and the processor bus.

READ/WRITE LOGIC

The read/write logic accepts processor data and stores it in its Initialization Command Word (ICW) and Operation Command Word (OCW) registers. It also controls the transfer of the Status Data to the processor's data bus.

CHIP SELECT ($\overline{\text{CS}}$)

The μPD8259 is enabled when an active-low signal is received at this input. Reading or writing of the μPD8259 is inhibited when it is not selected.

WRITE ($\overline{\text{WR}}$)

This active-low signal instructs the μPD8259 to receive Command Data from the processor.

READ ($\overline{\text{RD}}$)

When an active-low signal is received on the $\overline{\text{RD}}$ input, the status of the Interrupt Request Register, In-Service Register, Interrupt Mask Register or binary code of the Interrupt Level is placed on the data bus.

INTERRUPT (INT)

The interrupt output from the μPD8259 is directly connected to the processor's INT input. The voltage levels of this output are compatible with the 8080's input voltage and timing requirements.

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register stores the bits for the individual interrupt bits to be masked. The IMR masks the data in the ISR. Lower priority lines are not affected by masking a higher priority line.

FUNCTIONAL DESCRIPTION (CONT.)

INTERRUPT ACKNOWLEDGE ($\overline{\text{INTA}}$)

The interrupt acknowledge signal is usually received from the 8228 (system controller for the 8080A). The system controller generates three $\overline{\text{INTA}}$ pulses to signal the 8259 to issue a 3-byte CALL instruction onto the data bus.

A_0

A_0 is usually connected to the processor's address bus. Together with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals it directs the loading of data into the command register or the reading of status data. The following table illustrates the basic operations performed. Note that it is divided into three functions: Input, Output and Bus Disable distinguished by the $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{CS}}$ inputs.

μPD8259 BASIC OPERATION						
A_0	D_4	D_3	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	PROCESSOR INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or IR → Data Bus ①
1			0	1	0	IMR → Data Bus
						PROCESSOR OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	Data Bus → OCW2
0	0	1	1	0	0	Data Bus → OCW3
0	1	X	1	0	0	Data Bus → ICW1
1	X	X	1	0	0	Data Bus → OCW1, ICW2, ICW3 ②
						DISABLE FUNCTION
X	X	X	1	1	0	Data Bus → 3-State
X	X	X	X	X	1	Data Bus → 3-State

Notes: ① The contents of OCW2 written prior to the READ operation governs the selection of the IRR, ISR or Interrupt Level.

② The sequencer logic on the μPD8259 aligns these commands in the proper order.

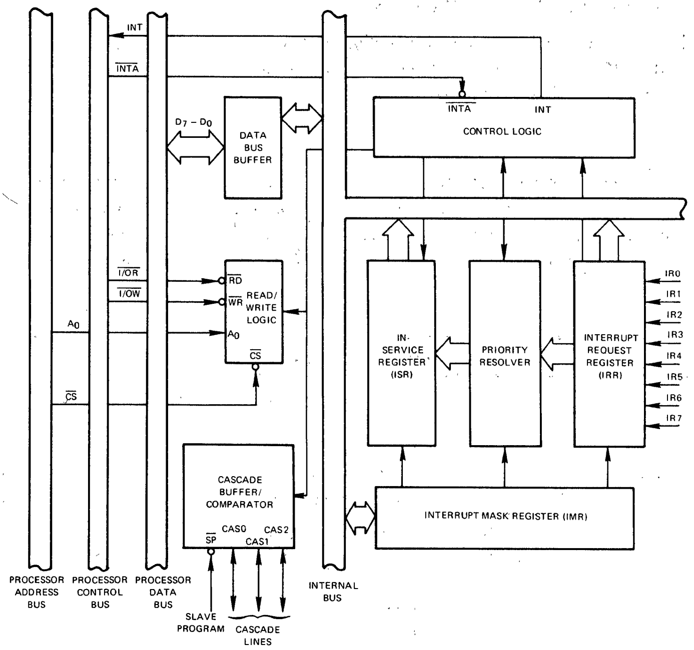
CASCADE BUFFER/COMPARATOR. (For Use in Multiple μPD8259 Array.)

The ID's of all μPD8259's are buffered and compared in the cascade buffer/ comparator. The master μPD8259 will send the ID of the interrupting slave device along the CAS0, 1, 2 lines to all slave devices. The cascade buffer/comparator compares its preprogrammed ID to the CAS0, 1, 2 lines. The next two $\overline{\text{INTA}}$ pulses strobe the preprogrammed, 2 byte CALL routine address onto the data bus from the slave whose ID matches the code on the CAS0, 1, 2 lines.

SLAVE PROGRAM ($\overline{\text{SP}}$). (For Use in Multiple μPD8259 Array.)

The interrupt capability can be expanded to 64 levels by cascading multiple μPD8259's in a master-plus-slaves array. The master controls the slaves through the CAS0, 1, 2 lines. The $\overline{\text{SP}}$ input to the device selects the CAS0-2 lines as either outputs ($\overline{\text{SP}}$=1) for the master or as inputs ($\overline{\text{SP}}$=0) for the slaves. For one device only the $\overline{\text{SP}}$ must be set to a logic "1" since it is functioning as a master.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

CAPACITANCE

$T_a = 25°C$; $V_{CC} = GND = 0V$

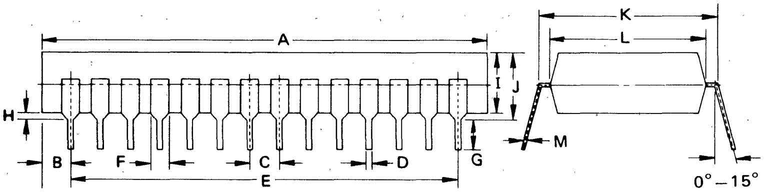
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	$f_c = 1$ MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured Pins Returned to V_{SS}

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

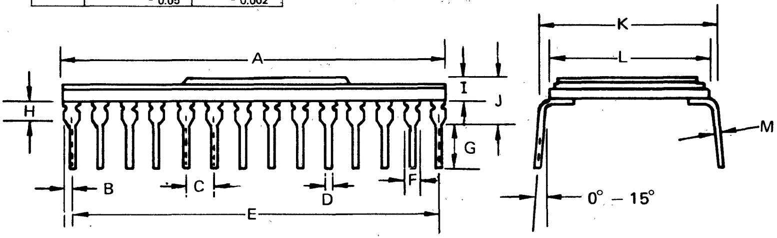
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5V	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Interrupt Output High Voltage	$V_{OH\text{-}INT}$	2.4			V	I_{OH} = −400 μA
		3.5			V	I_{OH} = −50 μA
Input Leakage Current for $IR_{0\text{-}7}$	I_{IL} ($IR_{0\text{-}7}$)			−300	μA	V_{IN} = 0V
				10	μA	V_{IN} = V_{CC}
Input Leakage Current for other Inputs	I_{IL}			10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LOL}			− 10	μA	V_{OUT} = 0.45 V
Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Supply Current	I_{CC}			100	mA	

PACKAGE OUTLINE
μPD8259C/D



(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.0 MAX	1.41 MAX
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

AC CHARACTERISTICS

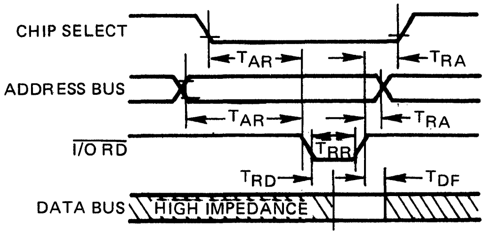
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		8259		8259-5			
		MIN	MAX	MIN	MAX		
READ							
$\overline{CS}$/A_0 Stable Before $\overline{RD}$ or $\overline{INTA}$	t_{AR}	50		50		ns	
$\overline{CS}$/A_0 Stable After $\overline{RD}$ or $\overline{INTA}$	t_{RA}	50		30		ns	
$\overline{RD}$ Pulse Width	t_{RR}	420		300		ns	
Data Valid From $\overline{RD}$/$\overline{INTA}$	t_{RD}		300		200	ns	①
Data Float After $\overline{RD}$/$\overline{INTA}$	t_{DF}	20	200	20	100	ns	①
WRITE							
A_0 Stable Before $\overline{WR}$	t_{AW}	50		50		ns	
A_0 Stable After $\overline{WR}$	t_{WA}	20		30		ns	
$\overline{CS}$ Stable Before $\overline{WR}$	t_{CW}	50				ns	
$\overline{CS}$ Stable After $\overline{WR}$	t_{WC}	20				ns	
$\overline{WR}$ Pulse Width	t_{WW}	400		300		ns	
Data Valid to $\overline{WR}$ (T.E.)	t_{DW}	300		250		ns	
Data Valid After $\overline{WR}$	t_{WD}	40		30		ns	
OTHER							
Width of Interrupt Request Pulse	t_{IW}	100		100		ns	
INT ↑ After IR ↑	t_{INT}	400		350		ns	
Cascade Line Stable After $\overline{INTA}$ ↑	t_{IC}	400		400		ns	

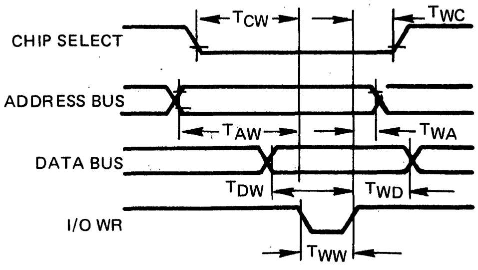
Note: ① For μPD8259: C_L = 100 pf; for μPD8259-5: C_L = 150 pf

TIMING WAVEFORMS

READ

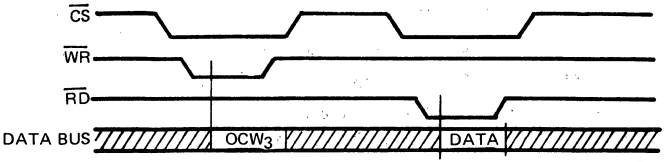


WRITE

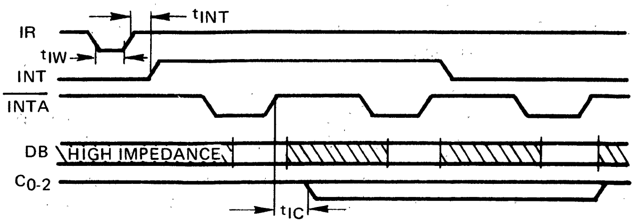


TIMING WAVEFORMS (CONT.)

READ STATUS/POLL MODE

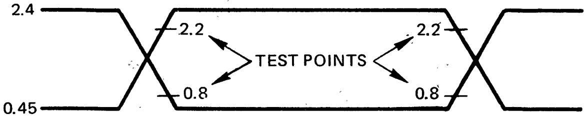


OTHER

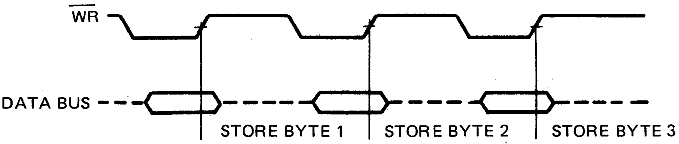


Note: IR must stay "high" at least until the leading edge of 1st $\overline{\text{INTA}}$.

INPUT WAVEFORMS FOR AC TESTS



INITIALIZATION SEQUENCE



DETAILED OPERATIONAL DESCRIPTION

The μPD8259 derives its versatility from its programmable interrupt modes and its ability to jump to any memory address through programmable CALL instructions. The following sequence demonstrates how the μPD8259 interacts with the processor.

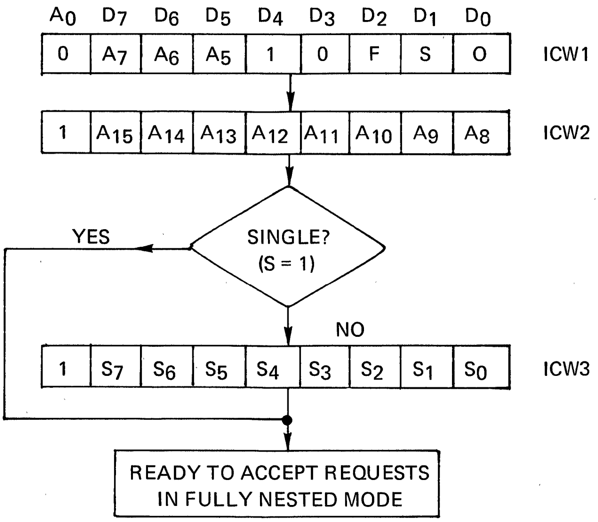
1. An interrupt or interrupts appearing on $IR_{0\text{-}7}$ sets the corresponding IR bit(s) high. This in turn sets the corresponding IRR bit(s) high.
2. Once the IRR bit(s) has been set, the μPD8259 will resolve the priorities according to the preprogrammed interrupt algorithm. It then issues an INT signal to the processor.
3. The processor group issues an $\overline{\text{INTA}}$ to the μPD8259 when it receives the INT.
4. The $\overline{\text{INTA}}$ input to the μPD8259 from the processor group sets the highest priority ISR bit and resets the corresponding IRR bit. The $\overline{\text{INTA}}$ also signals the μPD8259 to issue an 8-bit CALL instruction op-code (11001101) onto its Data bus lines.
5. The CALL instruction code instructs the processor group to issue two more $\overline{\text{INTA}}$ pulses to the μPD8259.
6. The two $\overline{\text{INTA}}$ pulses signal the μPD8259 to place its preprogrammed interrupt vector address onto the Data bus. The first $\overline{\text{INTA}}$ releases the low-order 8-bits of the address and the second $\overline{\text{INTA}}$ releases the high-order 8-bits.
7. The μPD8259's CALL instruction sequence is complete. A preprogrammed EOI (End-of-Interrupt) command is issued to the μPD8259 at the end of an interrupt service routine to reset the ISR bit and allow the μPD8259 to service the next interrupt.

PROGRAMMING THE μPD8259

Two types of command words are required from the processor to fully define the operating modes of the μPD8259.

1. **Initialization Command Words (ICWs)**

   Each μPD8259 in the interrupt array must be initialized prior to normal operation. The initialization is performed by a 2 or 3-byte sequence clocked by $\overline{\text{WR}}$ pulses. Figure 1 shows this sequence. (Refer to Figure 2 for bit definitions.)



INITIALIZATION SEQUENCE – FIGURE 1.

PROGRAMMING THE μPD8259 (CONT.)

2. Operation Command Words (OCWs)

The operation command words are used to program the various interrupt algorithms listed below:

- Fully Nested Mode
- Rotating Priority Mode
- Special Mask Mode
- Polled Mode

Once the μPD8259 has been initialized, OCWs can be written at any time.

INITIALIZATION COMMAND WORDS 1 and 2 (ICW1 and ICW2)

When $A_0 = 0$ and $D_4 = 1$ in a command to the μPD8259, together with $\overline{CS} = 0$, it is recognized as Initialization Command Word 1. This is the start of the initialization sequence and causes the following to occur:

- The Interrupt Request edge-sense circuitry is reset so that an input must make a low-to-high transition to generate its interrupt.
- The initialization sequence clears Interrupt Mask Register to all unmasked and resets the Special Mask Mode and Status Read Flip-Flops.
- IR_7 input is set to priority 7.

There are eight equally-spaced base vector addresses in memory for the eight interrupt inputs. The interval between the base vector addresses can be programmed to be either four or eight requiring 32 or 64 bytes in memory, respectively. The following shows how the address format is mapped onto the Data bus.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

DEFINED BY D5-7 OF ICW1

AUTOMATICALLY INSERTED BY μPD8259

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

DEFINED BY ICW2

The μPD8259 automatically defines $A_{0\text{-}4}$ with a separate address for each interrupt input. The base vector addresses $A_{15\text{-}6}$ are programmed by ICW1 and ICW2. A_5 is either defined by the μPD8259 if the address interval is eight or must be user-defined if the interval is 4. The 8-byte CALL interval is consistent with 8080A processor RESTAR instruction software. The 4-byte CALL interval can be used for a compact jump table. Refer to Figure 4 for a table of address formats.

The following is an example of an interrupt acknowledge sequence. The μPD8259 has been programmed for a CALL address (base vector address) interval of eight (F = 0) and there is an interrupt appearing on IR_4. The 3-byte sequence is strobed out to the Data bus by three $\overline{INTA}$ pulses.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1ST $\overline{INTA}$	1	1	0	0	1	1	0	1	CALL CODE
2ND $\overline{INTA}$	A_7	A_6	1	0	0	0	0	0	LOWER ROUTINE ADDRESS (FROM FIGURE 4)
3RD $\overline{INTA}$	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	HIGHER ROUTINE ADDRESS

INITIALIZATION COMMAND WORD 3 (ICW3) ①

It is only necessary to program ICW3 when there are multiple μPD8259s in the interrupt array, i.e., S = 0. There are two types of ICW3s. The first is for programming the master μPD8259. The second is for the slaves.

1. ICW3-Master μPD8259. A "1" is set in S$_{0-7}$ for each corresponding slave in the interrupt array. The S$_{0-7}$ bits, together with $\overline{SP}$ = 1, instructs the cascade buffer/comparator to send the ID of the interrupting slave on the CAS0,1,2 lines.
2. ICW3-SLAVE μPD8259(s). Bits D$_7$-D$_3$ are "don't care" bits and have no effect on ICW3. The ID of each slave is programmed by bits D$_{0-2}$ (ID$_{0,1,2}$). Once the master μPD8259 has sent out the first byte of the CALL sequence, the slave device(s) with their $\overline{SP}$ inputs set to Logic 0, compare their IDs appearing on the CAS0,1,2 lines through the cascade buffer/comparator. The slave whose ID matches the CAS0,1,2 code then issues bytes 2 and 3 of the CALL sequence.

OPERATIONAL COMMAND WORDS (OCWs) ②

Once the μPD8259 has been programmed with Initialization Command Words, it can now be programmed for the appropriate interrupt algorithm by the Operation Command Words. Interrupt algorithms in the μPD8259 can be changed at any time during program operation by issuing another set of Operation Command Words. The following sections describe the various algorithms available and their associated OCWs.

INTERRUPT MASKS

The individual Interrupt Request input lines are maskable by setting the corresponding bits in the Interrupt Mask Register to a logic "1" through OCW1. The actual masking is performed upon the contents of the In-Service Register (e.g., if Interrupt Request line 3 is to be masked, then only bit 3 of the IMR is set to logic "1." The IMR in turn acts upon the contents of the ISR to mask bit 3). Once the μPD8259 has acknowledged an interrupt, i.e., the μPD8259 has sent an INT signal to the processor and the system controller has sent it an $\overline{INTA}$ signal, the interrupt input, although it is masked, will inhibit lower priority requests from being acknowledged. There are two means of enabling these lower priority interrupt lines. The first is by issuing an End-of-Interrupt (EOI) through Operation Command Word 2 (OCW2), thereby resetting the appropriate ISR bit. The second approach is to select the Special Mask Mode through OCW3. The Special Mask Mode (SMM) and End-of-Interrupt (EOI) will be described in more detail further on.

FULLY NESTED MODE

The fully nested mode is the μPD8259's basic operating mode. It will operate in this mode after the initialization sequence, requiring no Operation Command Words for formatting. Priorities are set IR$_0$ through IR$_7$ with IR$_0$ the highest priority. After the interrupt has been acknowledged by the processor and system controller, only higher priorities will be serviced. Upon receiving an $\overline{INTA}$, the priority resolver determines the priority of the interrupt, the corresponding ISR bit is set, and the vector address is output to the Data bus. The EOI command resets the corresponding ISR bit at the end of its service routine.

Notes: ① Reference Figure 2
② Reference Figure 3

OPERATIONAL COMMAND WORDS (CONT.)

ROTATING PRIORITY MODE COMMANDS

The two variations of Rotating Priorities are the Auto Rotate and Specific Rotate modes. These two modes are typically used to service interrupting devices of equivalent priorities.

1. Auto Rotate Mode

   Programming the Auto Rotate Mode through OCW2 assigns priorities 0-7 to the interrupt request input lines. Interrupt line IR_0 is set to the highest priority and IR_7 to the lowest. Once an interrupt has been serviced it is automatically assigned the lowest priority. That same input must then wait for the devices ahead of it to be serviced before it can be acknowledged again. The Auto Rotate Mode is selected by programming OCW2 in the following way (refer to Figure 3): set Rotate Priority bit "R" to a logic "1"; program EOI to a logic "1" and SEOI to a logic "0." The EOI and SEOI commands are discussed further on. The following is an example of the Auto Rotate Mode with devices requesting interrupts on lines IR_2 and IR_5.

   Before Interrupts are Serviced:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	1	0	0
Priority Status Register	IR_7	IR_6	IR_5	IR_4	IR_3	IR_2	IR_1	IR_0

→ Highest Priority

   According to the Priority Status Register, IR_2 has a higher priority than IR_5 and will be serviced first.

   After Servicing:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	0	0	0
Priority Status Register	IR_2	IR_1	IR_0	IR_7	IR_6	IR_5	IR_4	IR_3

→ Highest Priority

   At the completion of IR_2's service routine the corresponding In-Service Register bit, IS_2 is reset to "0" by the preprogrammed EOI command. IR_2 is then assigned the lowest priority level in the Priority Status Register. The μPD8259 is now ready to service the next highest interrupt, which in this case, is IR_5.

2. Specific Rotate Mode

   The priorities are set by programming the lowest level through OCW2. The μPD8259 then automatically assigns the highest priority. If, for example, IR_3 is set to the lowest priority (bits L_2, L_1, L_0 form the binary code of the bottom priority level), then IR_4 will be set to the highest priority. The Specific Rotate Mode is selected by programming OCW2 in the following manner: set Rotate Priority bit "R" to a logic "1," program EOI to a logic "0," SEOI to a logic "1" and L_2, L_1, L_0 to the lowest priority level. If EOI is set to a logic "1," the ISR bit defined by L_2, L_1, L_0 is reset.

END-OF-INTERRUPT (EOI) AND SPECIFIC END-OF-INTERRUPT (SEOI)

The End-of-Interrupt or Specific End-of-Interrupt command must be issued to reset the appropriate In-Service Register bit before the completion of a service routine. Once the ISR bit has been reset to logic "0," the μPD8259 is ready to service the next interrupt.

Two types of EOIs are available to clear the appropriate ISR bit depending on the μPD8259's operating mode.

1. Non-Specific End-of-Interrupt (EOI)
   When operating in interrupt modes where the priority order of the interrupt inputs is preserved (e.g., fully nested mode), the particular ISR bit to be reset at the completion of the service routine can be determined. A non-specific EOI command will automatically reset the highest priority ISR bit of those set. The highest priority ISR bit must necessarily be the interrupt being serviced and must necessarily be the service subroutine returned from.
2. Specific End-of-Interrupt (SEOI)
   When operating in interrupt modes where the priority order of the interrupt inputs is not preserved (e.g., rotating priority mode) the last serviced interrupt level may not be known. In these modes a Specific End-of-Interrupt must be issued to clear the ISR bit at the completion of the interrupt service routine. The SEOI is programmed by setting the appropriate bits in OCW3 (Figure 2) to logic "1"s. Both the EOI and SEOI bits of OCW3 must be set to a logic "1" with L_2, L_1, L_0 forming the binary code of the ISR bit to be reset.

SPECIAL MASK MODE

Setting up an interrupt mask through the Interrupt Mask Register (refer to Interrupt Mask Register section) by setting the appropriate bits in OCW1 to a logic "1" will inhibit lower priority interrupts from being acknowledged. In applications requiring that the lower priorities be enabled while the IMR is set, the Special Mask Mode can be used. The SMM is programmed in OCW3 by setting the appropriate bits to a logic "1." Once the SMM is set, the μPD8259 remains in this mode until it is reset. The Special Mask Mode does not affect the higher priority interrupts.

POLLED MODE

In the Poll Mode the processor must be instructed to disable its interrupt input (INT). Interrupt service is initiated through software by a Poll Command. The Poll Mode is programmed by setting the Poll Mode bit in OCW3 (P = 1), during a $\overline{WR}$ pulse. The following $\overline{RD}$ pulse is then considered as an interrupt acknowledge. If an interrupt input is present, that $\overline{RD}$ pulse sets the appropriate ISR bit and reads the interrupt priority level. The Poll Mode is a one-time operation and must be programmed through OCW3 before every read. The word strobed onto the Data bus during Poll Mode is of the form:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	X	X	X	X	W_2	W_1	W_0

where: I = 1 if there is an interrupt requesting service
= 0 if there are no interrupts

W_{2-0} forms the binary code of the highest priority level of the interrupts requesting service

The Poll Mode can be used when an interrupt service routine is common to several interrupt inputs. The $\overline{INTA}$ sequence is no longer required offering a saving in ROM space. The Poll Mode can also be used to expand the number of interrupts beyond 64.

READING μPD8259 STATUS

The following major registers' status is available to the processor by appropriately formatting OCW3 and issuing a $\overline{RD}$ command.

INTERRUPT REQUEST REGISTER (8-BITS)

The Interrupt Request Register stores the interrupt levels awaiting acknowledgement. Once it has been acknowledged, the highest priority in-service bit is reset. (Note that the Interrupt Mask Register has no effect on the IRR.) A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. The bits which determine whether the IRR and ISR are being read from are RIS and ERIS. To read contents of the IRR, ERIS must be logic "1" and RIS a logic "0."

IN-SERVICE REGISTER (8-BITS)

The In-Service Register stores the priorities of the interrupt levels being serviced. Assertion of an End-of-Interrupt (EOI) updates the ISR to the next priority level. A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. Both ERIS and RIS should be set to a logic "1."

INTERRUPT MASK REGISTER (8-BITS)

The Interrupt Mask Register holds mask data modifying interrupt levels. To read the IMR status a $\overline{WR}$ pulse preceding the $\overline{RD}$ is not necessary. The IMR data is available to the data bus when $\overline{RD}$ is asserted with A_0 at a logic "1."

A single OCW3 is sufficient to enable successive status reads providing it is of the same register. A status read is over-ridden by the Poll Mode where bits P and ERIS of OCW3 are set to a logic "1."

CASCADING MULTIPLE μPD8259s

If more than eight interrupt levels are required, multiple μPD8259s can be cascaded with one master and up to eight slaves, to accommodate up to 64 levels of interrupt.

As shown in Figure 5, the master device directs the appropriate slave to release its CALL address through its three cascade lines (CAS0,1,2).

The INT output of the slave devices go to the IR inputs of the master device. The master μPD8259's INT output is connected to the processor's control bus. When the slave device signals the master that it has acknowledged an interrupt, the master issues an 8080A CALL Op-code at the first $\overline{INTA}$ pulse. The master then signals that slave device (via CAS0,1,2) to issue the appropriate CALL address during the second and third $\overline{INTA}$ pulses.

The slave address code is present on cascade lines 0,1,2 (active-high logic) from the trailing edge of the first $\overline{INTA}$ to the trailing edge of the third $\overline{INTA}$. Each device in the μPD8259 array must be individually initialized and can be programmed in different operating modes. Two End-of-Interrupt commands must be issued for the master and its corresponding slave. An address decoder is used to drive the Chip Select inputs for each μPD8259 in the array. The Slave Program ($\overline{SP}$) input must be held at a logic "0" level for each slave device and held at logic "1" level for the master. The $\overline{SP}$ input selects the Cascade lines as either inputs ($\overline{SP}$ = 0) or outputs ($\overline{SP}$ = 1).

INITIALIZATION COMMAND WORD FORMAT

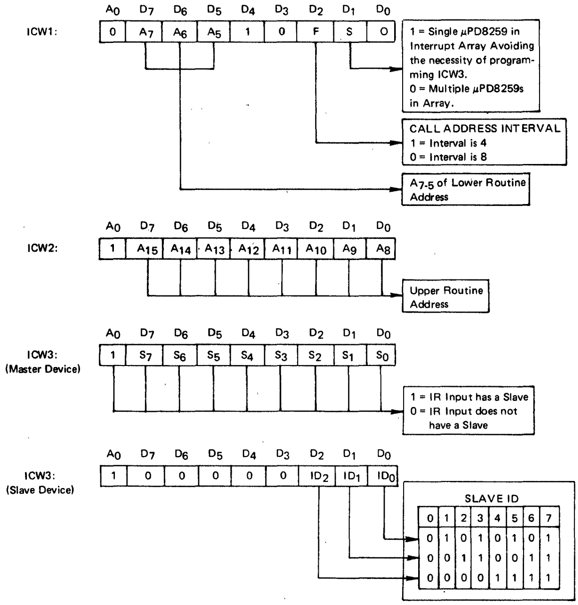


FIGURE 2

OPERATION COMMAND WORD FORMAT

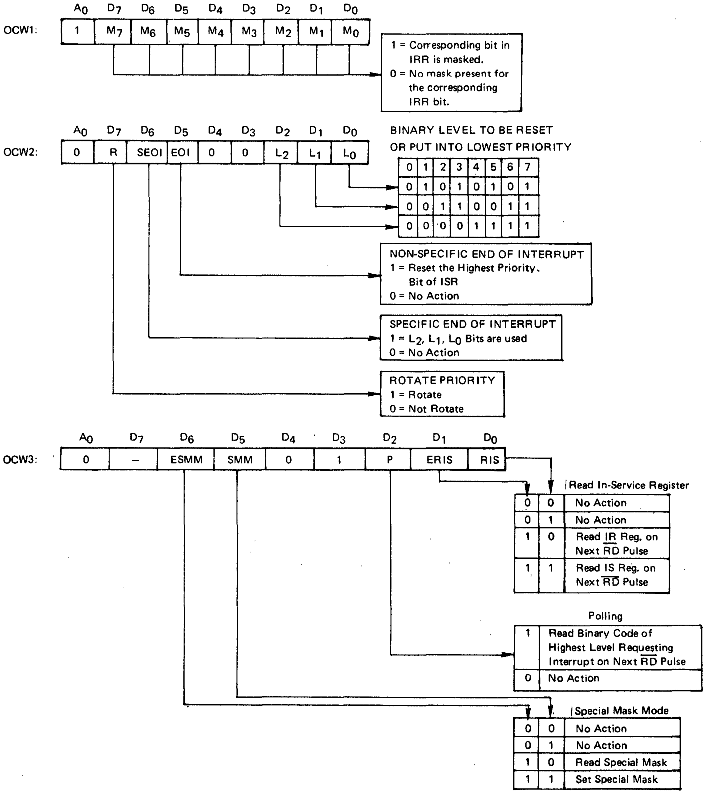


FIGURE 3

SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

	A_0	D_4	D_3				
OCW1	1	X	X	M_7-M_0			IMR (Interrupt Mask Register) $\overline{WR}$ loads IMR data while $\overline{RD}$ reads status
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action
				0	0	1	Non-Specific End-of-Interrupt
				0	1	0	No Action
				0	1	1	Specific-End-of-Interrupt L_2, L_1, L_0 forms binary representation of level to be reset.
				1	0	0	No Action
				1	0	1	Rotate Priority at End-of-Interrupt (Auto Mode)
				1	1	0	Rotate Priority, L_2, L_1, L_0 specifies bottom priority without End-of-Interrupt
				1	1	1	Rotate Priority at End-of-Interrupt (Specific Mode). L_2, L_1, L_0 specifies bottom priority, and its In-Service Register bit is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not affected
				0	1		
				1	0		Reset Special Mask
				1	1		Set Special Mask
				ERIS	RIS		
				0	0		No Action
				0	1		
				1	0		Read IR Register Status
				1	1		Read IS Register Status

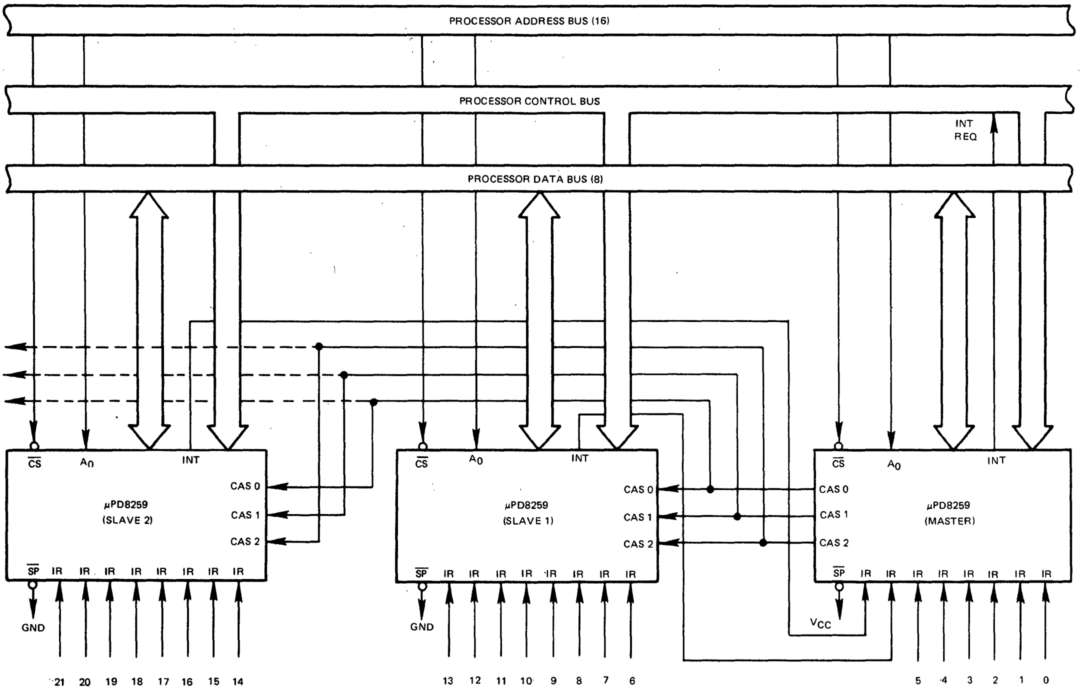
LOWER MEMORY INTERRUPT VECTOR ADDRESS

	INTERVAL = 4								INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0	A_7	A_6	0	0	0	0	0	0

FIGURE 4

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259s.

CASCADING THE μPD8259



INSTRUCTION SET

Instruction Number	Mnemonic	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operation Description
1	ICW1 A	0	A_7	A_6	A_5	1	0	1	1	0	Byte 1 Initialization, Format = 4, Single
2	ICW1 B	0	A_7	A_6	A_5	1	0	1	0	0	Byte 1 Initialization, Format = 4, Not Single
3	ICW1 C	0	A_7	A_6	A_5	1	0	0	1	0	Byte 1 Initialization, Format = 8, Single
4	ICW1 D	0	A_7	A_6	A_5	1	0	0	0	0	Byte 1 Initialization, Format = 8, Not Single
5	ICW2	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	Byte 2 Initialization (Address No. 2)
6	ICW3 M	1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Byte 2 Initialization – MASTER
7	ICW3 S	1	0	0	0	0	0	S_2	S_1	S_0	Byte 3 Initialization – SLAVE
8	OCW1	1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0	Load Mask Register, Read Mask Register
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non-Specific EOI
10	OCW2 SE	0	0	1	1	0	0	L_2	L_1	L_0	Specific EOI, L_2, L_1, L_0 Code of IS to be Reset
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode)
12	OCW2 RSE	0	1	1	1	0	0	L_2	L_1	L_0	Rotate at EOI (Specific Mode). L_2, L_1, L_0 Code of Line to be Reset and Selected as Bottom Priority.
13	OCW2 RS	0	1	1	0	0	0	L_2	L_1	L_0	L_2, L_1, L_0 – Code of Bottom Priority Line.
14	OCW3 P	0	–	0	0	0	1	1	0	0	Poll Mode
15	OCW3 RIS	0	–	0	0	0	1	0	1	1	Read IS Register
16	OCW3 RR	0	–	0	0	0	1	0	1	0	Read Requests Register
17	OCW3 SM	0	–	1	1	0	1	0	0	0	Set Special Mask Mode
18	OCW3 RSM	0	–	1	0	0	1	0	0	0	Reset Special Mask Mode

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259s.

NEC Microcomputers, Inc.

NEC
μPD8279-5

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

DESCRIPTION

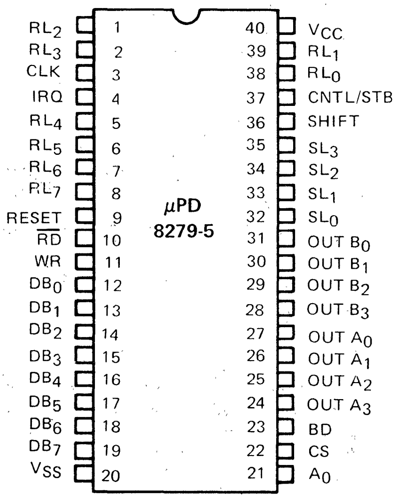
The μPD8279-5 is a programmable keyboard and display Input/Output device. It provides the user with the ability to display data on alphanumeric segment displays or simple indicators. The display RAM can be programmed as 16 x 8 or a dual 16 x 4 and loaded or read by the host processor. The display can be loaded with right or left entry with an auto-increment of the display RAM address.

The keyboard interface provides a scanned signal to a 64 contact key matrix expandable to 128. General sensors or strobed keys may also be used. Keystrokes are stored in an 8 character FIFO and can be either 2 key lockout or N key rollover. Keyboard entries generate an interrupt to the processor.

FEATURES

- Programmable by Processor
- 32 HEX or 16 Alphanumeric Displays
- 64 Expandable to 128 Keyboard
- Simultaneous Keyboard and Display
- 8 Character Keyboard – FIFO
- 2 Key Lockout or N Key Rollover
- Contact Debounce
- Programmable Scan Timer
- Interrupt on Key Entry
- Single +5 Volt Supply
- Fully Compatible with 8080A, 8085A, μPD780 (Z80™)
- Available in 40 Pin Plastic Package

PIN CONFIGURATION



PIN NAMES

DB_{0-7}	Data Bus (Bi-directional)
CLK	Clock Input
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Buffer Address
IRQ	Interrupt Request Output
SL_{0-3}	Scan Lines
RL_{0-7}	Return Lines
SHIFT	Shift Input
CNTL/STB	Control/Strobe Input
OUT A_{0-3}	Display (A) Outputs
OUT B_{0-3}	Display (B) Outputs
$\overline{BD}$	Bland Display Output

TM: Z80 is a registered trademark of Zilog.

FUNCTIONAL DESCRIPTION

The μPD8279-5 has two basic functions: 1) to control displays to output and 2) to control a keyboard for input. Its specific purpose is to unburden the host processor from monitoring keys and refreshing displays. The μPD8279-5 is designed to directly interface the microprocessor bus. The microprocessor must program the operating mode to the μPD8279-5, these modes are as follows:

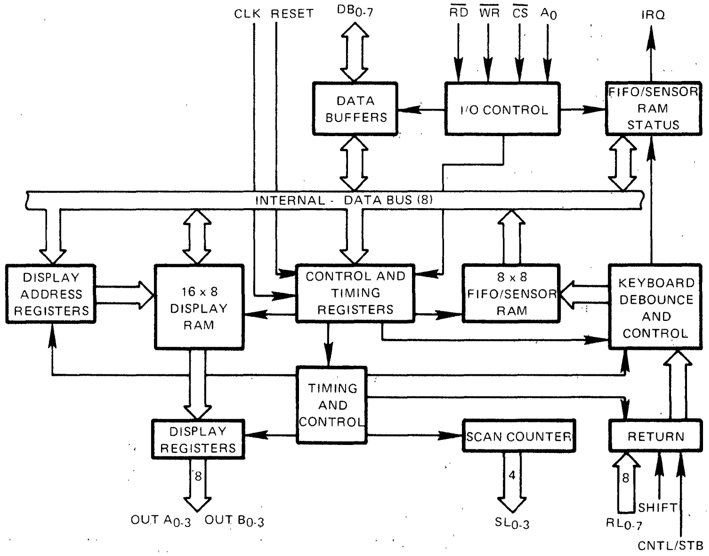
Output Modes

- 8 or 16 Character Display
- Right or Left Entry

Input Modes

- Scanned Keyboard with Encoded 8 x 8 x 4 Key Format or Decoded 4 x 8 x 8 Scan Lines.
- Scanned Sensor Matrix with Encoded 8 x 8 or Decoded 4 x 8 Scan Lines.
- Strobed Input.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts①
All Input Voltages	-0.5 to +7 Volts①
Supply Voltages	-0.5 to +7 Volts①
Power Dissipation	1W

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$^*T_a = 25°C$

PIN IDENTIFICATION

PIN			DESCRIPTION
NO.	SYMBOL	NAME	
1, 2, 5, 6, 7, 8, 38, 39	RL_{0-7}	Return Lines	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
3	CLK	Clock	Clock from system used to generate internal timing.
4	IRQ	Interrupt Request	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
9	Reset	Reset Input	A high signal on this pin resets the μPD8279-5.
10	$\overline{RD}$	Read Input	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
11	$\overline{WR}$	Write Input	
12-19	DB_{0-7}	Data Bus	Bi-Directional data bus. All data and commands between the processor and the μPD8279-5 are transmitted on these lines.
20	V_{SS}	Ground Reference	Power Supply Ground
21	A_0	Buffer Address	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
22	$\overline{CS}$	Chip Select	Chip Select. A low on this pin enables the interface functions to receive or transmit.
23	$\overline{BD}$	Blank Display Output	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.
24-27	OUT A_{0-3}	Display A Outputs	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4-bit ports may be blanked independently. These two ports may also be considered as one 8-bit port.
28-31	OUT B_{0-3}	Display B Outputs	
32-35	SL_{0-3}	Scan Lines	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
36	Shift	Shift Input	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
37	CNTL/STB	Control/ Strobe Input	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in Strobed input mode (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
40	V_{CC}	+5V Input	Power Supply Input

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$.

DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage for Shift, Control and Return Lines	V_{IL1}	-0.5		1.4	V	
Input Low Voltage (Others)	V_{IL2}	-0.5		0.8	V	
Input High Voltage for Shift, Control and Return Lines	V_{IH1}	2.2			V	
Input High Voltage (Others)	V_{IH2}	2.0			V	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.2$ mA
Output High Voltage on Interrupt Line	V_{OH}	3.5			V	$I_{OH} = -400\ \mu A$
Input Current on Shift, Control and Return Lines	I_{IL1}			+10 -100	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$
Input Leakage Current (Others)	I_{IL2}			±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Float Leakage	I_{OFL}			±10	μA	$V_{OUT} = V_{CC}$ to 0V
Power Supply Current	I_{CC}			120	mA	

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}	5		10	pF	$V_{IN} = V_{CC}$
Output Capacitance	C_{OUT}	10		20	pF	$V_{OUT} = V_{CC}$

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

AC CHARACTERISTICS

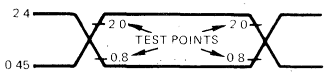
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable Before $\overline{\text{READ}}$	t_{AR}	0			ns	
Address Hold Time for $\overline{\text{READ}}$	t_{RA}	0			ns	
$\overline{\text{READ}}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{\text{READ}}$	t_{RD}			150	ns	$C_L = 150$ pF
Address to Data Valid	t_{AD}			250	ns	$C_L = 150$ pF
$\overline{\text{READ}}$ to Data Floating	t_{DF}	10		100	ns	
Read Cycle Time	t_{RCY}	1			μs	
WRITE						
Address Stable Before $\overline{\text{WRITE}}$	t_{AW}	0			ns	
Address Hold Time for $\overline{\text{WRITE}}$	t_{WA}	0			ns	
$\overline{\text{WRITE}}$ Pulse Width	t_{WW}	250			ns	
Data Set Up Time for $\overline{\text{WRITE}}$	t_{DW}	150			ns	
Data Hold Time for $\overline{\text{WRITE}}$	t_{WD}	0			ns	
OTHER						
Clock Pulse Width	$t_{\phi W}$	120			ns	
Clock Period	t_{CY}	320			ns	

GENERAL TIMING

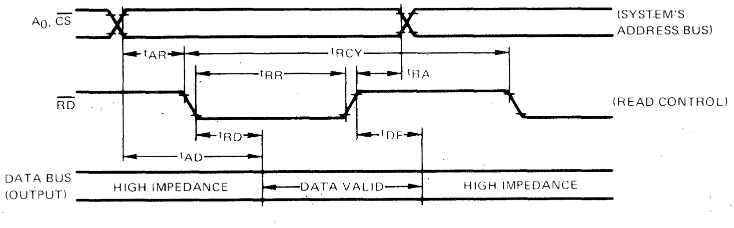
Keyboard Scan Time:	5.1 ms	Digit-on Time:	480 μs
Keyboard Debounce Time:	10.3 ms	Blanking Time:	160 μs
Key Scan Time:	80 μs	Internal Clock Cycle:	10 μs
Display Scan Time:	10.3 ms		

TIMING WAVEFORMS

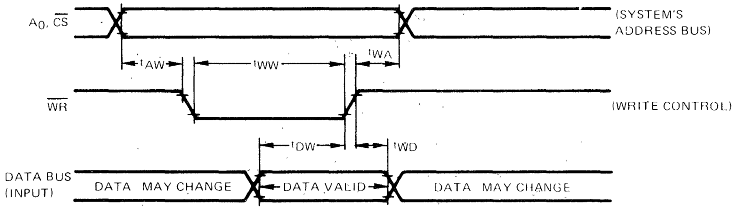
INPUT FOR AC TESTS



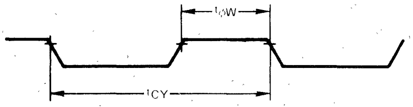
READ



WRITE



CLOCK INPUT



OPERATIONAL DESCRIPTION

The following is a description of each section of the μPD8279-5. See the block diagram for functional reference.

I/O Control and Data Buffers

Communication to and from the μPD8279-5 is performed by selecting $\overline{\text{CS}}$, A_0, $\overline{\text{RD}}$ and $\overline{\text{WR}}$. The type of information written or read by the processor is selected by A_0. A logic 0 states that information is data while a 1 selects command or status. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ select the direction by which the transfer occurs through the Data Buffers. When the chip is deselected ($\overline{\text{CS}}$ = 1) the bi-directional Data Buffers are in a high impedance state thus enabling the μPD8279-5 to be tied directly to the processor data bus.

Timing Registers and Timing Control

The Timing Registers store the display and keyboard modes and other conditions programmed by the processor. The timing control contains the timing counter chain. One counter is a divide by N scaler which may be programmed to match the processor cycle time. The scaler must take a value between 2 and 31 in binary. A value which scales the internal frequency to 100 KHz gives a 5.1 ms scan time and 10.3 ms switch debounce. The other counters divide down to make key, row matrix and display scans.

Scan Counter

The scan counter can operate in either the encoded or decoded mode. In the encoded mode, the counter provides a count which must be decoded to provide the scan lines. In the decoded mode, the counter provides a 1 out of 4 decoded scan. In the encoded mode the scan lines are active high and in the decoded mode they are active low.

Return Buffers, Keyboard Debounce and Control

The eight return lines are buffered and latched by the return buffers. In the keyboard mode these lines are scanned sampling for key closures in each row. If the debounce circuit senses a closure, about 10 ms are timed out and a check is performed again. If the switch is still pressed, the address of the switch matrix plus the status of shift and control are written into the FIFO. In the scanned sensor mode, the contents of return lines are sent directly to the sensor RAM (FIFO) each key scan. In the strobed mode, the transfer takes place on the rising edge of CNTL/STB.

FIFO/Sensor RAM and Status

This section is a dual purpose 8 x 8 RAM. In strobe or keyboard mode it is a FIFO. Each entry is pushed into the FIFO and read in order. Status keeps track of the number of entries in the FIFO. Too many reads or writes to the FIFO will be treated as an error condition. The status logic generates an IRQ whenever the FIFO has an entry. In the sensor mode the memory is a sensor RAM which detects changes in the status of a sensor. If a change occurs, the IRQ is generated until the change is acknowledged.

Display Address Registers and Display RAM

The Display Address Register contains the address of the word being read or written by the processor, as well as the word being displayed. This address may be programmed to auto-increment after each read or write. The display RAM may be read by the processor any time after the mode and address is set. Data entry to the display RAM may be set to either right or left entry.

COMMAND OPERATION

The commands programmable to the μPD8279-5 via the data bus with $\overline{CS}$ active (0) and A_0 high are as follows:

Keyboard/Display Mode Set

0	0	0	D	D	K	K	K

MSB LSB

Display Mode:

DD		
0	0	8-8-bit character display — Left entry
0	1①	16-8 bit character display — Left entry
1	0	8-8 bit character display — Right entry
1	1	16-8 bit character display — Right entry

Note: ① Power on default condition

Keyboard Mode:

KKK			
0	0	0	Encoded Scan — 2 Key Lockout
0	0	1	Decoded Scan — 2 Key Lockout
0	1	0	Encoded Scan — N Key Rollover
0	1	1	Decoded Scan — N Key Rollover
1	0	0	Encoded Scan-Sensor Matrix
1	0	1	Decoded Scan-Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value between 2 and 31 this prescaler divides the external clock by PPPPP to develop its internal frequency. After reset, a default value of 31 is generated.

Read FIFO/Sensor RAM

0	1	0	AI	X	A	A	A

$A_0 = 0$

A_I is the auto-increment flag. AAA is the row to be read by the processor. The read command is accomplished with ($\overline{CS} \cdot RD \cdot \overline{A0}$) by the processor. If A_I is 1, the row select counter will be incremented after each read. Note that auto-incrementing has no effect on the display.

Read Display RAM

0	1	1	AI	A	A	A	A

$A_0 = 0$

Where A_I is the auto-increment flag and AAAA is the character which the processor is about to read.

Write Display RAM

1	0	0	AI	A	A	A	A

where AAAA is the character the processor is about to write.

Display Write Inhibit Blanking

1	0	1	X	IW A	IW B	BL A	BL B

Where IWA and IWB are Inhibit Writing nibble A and B respectively, and BLA, BLB are blanking. When using the display as a dual 4-bit, it is necessary to mask one of the 4-bit halves to eliminate interaction between the two halves. This is accomplished with the IW flags. The BL flags allow the programmer to blank either half of the display independently. To blank a display formatted as a single 8-bit, it is necessary to set both BLA and BLB. Default after a reset is all zeros. All signals are active high (1).

COMMAND OPERATION (CONT.)

Clear

1	1	0	C_D	C_D	C_D	C_F	C_A

C_D	C_D	C_D	
1	0	X	All zeros
1	1	0	AB = 20_{16}
1	1	1	All ones
0	X	X	Disable clear display

This command is used to clear the display RAM, the FIFO, or both. The C_D options allow the user the ability to clear the display RAM to either all zeros or all ones.

C_F clears the FIFO.
C_A clears all.

Clearing the display takes one complete display scan. During this time the processor can't write to the display RAM.

C_F will set the FIFO empty flag and reset IRQ. The sensor matrix mode RAM pointer will then be set to row 0.

C_A is equivalent to C_F and C_D. The display is cleared using the display clear code specified and resets the internal timing logic to synchronize it.

End Interrupt/Error Mode Set

1	1	1	E	X	X	X	X

In the sensor matrix mode, this instruction clears IRQ and allows writing into RAM.

In N key rollover, setting the E bit to 1 allows for operating in the special Error mode. See Description of FIFO status.

FIFO Status

D_U	S/E	O	U	F	N	N	N

Where: D_U = Display Unavailable because a clear display or clear all command is in progress.

S/E = Sensor Error flag due to multiple closure of switch matrix.

O = FIFO Overrun since an attempt was made to push too many characters into the FIFO.

U = FIFO Underrun. An indication that the processor tried to read an empty FIFO.

F = FIFO Full Flag.

NNN = The Number of characters presently in the FIFO.

The FIFO Status is Read with A_0 high and $\overline{CS}$, $\overline{RD}$ active low.

The Display not available is an indication that the C_D or C_A command has not completed its clearing. The S/E flags are used to show an error in multiple closures has occurred. The O or U, overrun or underrun, flags occur when too many characters are written into the FIFO or the processor tries to read an empty FIFO. F is an indication that the FIFO is full and NNN is the number of characters in the FIFO.

Data Read

Data can be read during $A_0 = 0$ and when $\overline{CS}$, $\overline{RD}$ are active low. The source of the data is determined by the Read Display or Read FIFO commands.

Data Write

Data is written to the chip when A_0, $\overline{CS}$, and $\overline{WR}$ are active low. Data will be written into the display RAM with its address selected by the latest Read or Write Display command.

COMMAND OPERATION (CONT.)

Data Format

CNTL	SH	SCAN	RET

In the Scanned Key mode, the characters in the FIFO correspond to the above format where CNTL and SH are the most significant bits and the SCAN and return lines are the scan and column counters.

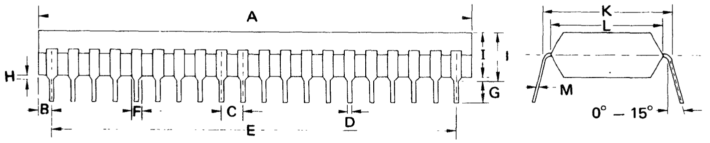
RL$_7$	RL$_6$	RL$_5$	RL$_4$	RL$_3$	RL$_2$	RL$_1$	RL$_0$

In the Sensor Matrix mode, the data corresponds directly to the row of the sensor RAM being scanned. Shift and control (SH, CNTL) are not used in this mode.

Control Address Summary

A$_0$	DATA MSB							LSB	
1	0	0	0	D	D	K	K	K	Keyboard Display Mode Set
1	0	0	1	P	P	P	P	P	Load Program Clock
0	0	1	0	A$_1$	X	A	A	A	Read FIFO/Sensor RAM
0	0	1	1	A$_1$	A	A	A	A	Read Display RAM
1	1	0	0	A$_1$	A	A	A	A	Write Display RAM
1	1	0	1	X	IW A	IW B	BL A	BL B	Display Write Inhibit/Blanking
1	1	1	0	C$_D$	C$_D$	C$_D$	C$_F$	C$_A$	Clear
1	1	1	1	E	X	X	X	X	End Interrupt/Error Mode Set
1	D$_U$	S/E	O	U	F	N	N	N	FIFO Status

PACKAGE OUTLINE
μPD8279C-5



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{-0.002}$

NEC Microcomputers, Inc.

NEC

μPD8355
μPD8755A*

16,384 BIT ROM WITH I/O PORTS
16,384 BIT EPROM WITH I/O PORTS*

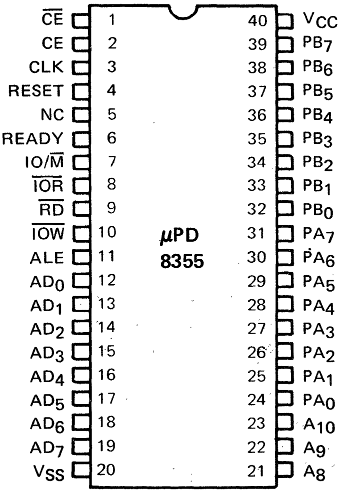
DESCRIPTION

The μPD8355 and the μPD8755A are μPD8085A Family components with the μPD8355 containing 2048 X 8 bits of mask ROM and the μPD8755A containing 2048 X 8 bits of mask EPROM for program development. Both components also contain two general purpose 8-bit I/O ports. They are housed in 40 pin packages, are designed to directly interface to the μPD8085A and are pin for pin compatible to each other.

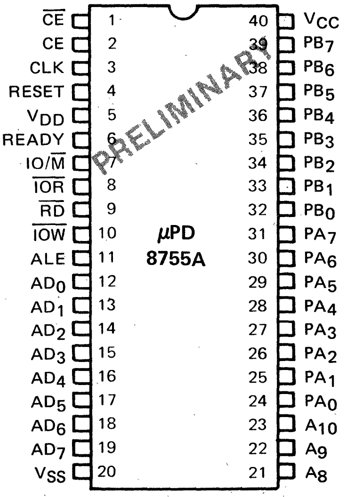
FEATURES

- 2048 X 8 Bits Mask ROM (μPD8355)
- 2048 X 8 Bits Mask EPROM (μPD8755A)
- 2 Programmable I/O Ports
- Single Power Supplies: +5V
- Directly Interfaces to the μPD8085A
- Pin for Pin Compatible
- μPD8755A: UV Eraseable and Electrically Programmable
- μPD8355 available in Plastic Package
- μPD8755A Available in Ceramic Package

PIN CONFIGURATIONS



NC: Not Connected



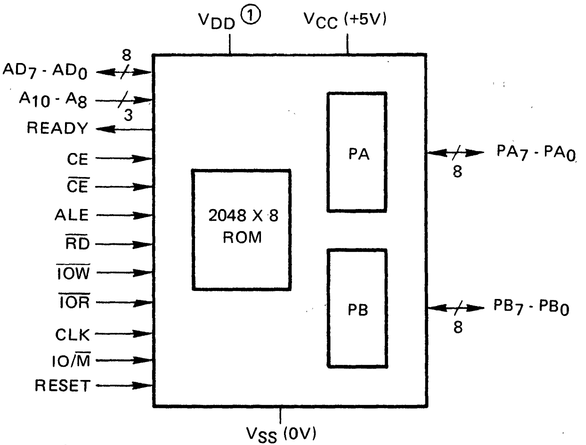
*All data pertaining to the μPD8755A is preliminary.

FUNCTIONAL DESCRIPTION

The μPD8355 and μPD8755A contain 16,384 bits of mask ROM and EPROM respectively, organized as 2048 X 8. The 2048 word memory location may be selected anywhere within the 64K memory space by using the upper 5-bits of address from the μPD8085A as a chip select.

The two general purpose I/O ports may be programmed input or output at any time. Upon power up, they will be reset to the input mode.

BLOCK DIAGRAM



Note: ① V_{DD} applies to μPD8755A only.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature (μPD8355) . . . . 0°C to +70°C
(μPD8755A) . . . . −10°C to +70°C
Storage Temperature (Ceramic Package) . . . . −65°C to +150°C
(Plastic Package) . . . . −40°C to +125°C
Voltage on Any Pin (μPD8355) . . . . −0.3 to +7 Volts ①
(μPD8755A) . . . . −0.5 to +7 Volts ①
Power Dissipation 1.5W

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$^*T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	$V_{CC} = 5.0V$ ①
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.5$	V	$V_{CC} = 5.0V$ ①
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2$ mA
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400$ μA
Input Leakage	I_{IL}			10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current	I_{LO}			±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
V_{CC} Supply Current	I_{CC}			180	mA	

Note: ① These conditions apply to μPD8355 only.

PIN IDENTIFICATION

PIN			
NO.	**SYMBOL**	**NAME**	**FUNCTION**
1,2	$\overline{CE}$, CE	Chip Enables	Enable Chip activity for memory or I/O
3	CLK	Clock Input	Used to Synchronize Ready
4	Reset	Reset Input	Resets PA and PB to all inputs
5 ①	NC	Not Connected	
5 ②	V_{DD}	Programming Voltage	Used as a programming voltage, tied to +5V normally
6	Ready	Ready Output	A tri-state output which is active during data direction register loading
7	IO/$\overline{M}$	I/O or Memory Indicator	An input signal which is used to indicate I/O or memory activity
8	IOR	I/O Read	I/O Read Strobe In
9	$\overline{RD}$	Memory Read	Memory Read Strobe In
10	$\overline{IOW}$	I/O Write	I/O Write Strobe In
11	ALE	Address Low Enable	Indicates information on Address/Data lines is valid
12-19	AD_0-AD_7	Low Address/Data Bus	Multiplexed Low Address and Data Bus
20	V_{SS}	Ground	Ground Reference
21-23	A_8-A_{10}	High Address	High Address inputs for ROM reading
24-31	PA_0-PA_7	Port A	General Purpose I/O Port
32-39	PB_0-PB_7	Port B	General Purpose I/O Port
40	V_{CC}	5V Input	Power Supply

Notes: ① μPD8355
② μPD8755A

I/O PORTS

I/O Port activity is controlled by performing I/O reads and writes to selected I/O port numbers. Any activity to and from the μPD8355 requires the chip enables to be active. This can be accomplished with no external decoding for multiple devices by utilizing the upper address lines for chip selects. ① Port activity is controlled by the following I/O addresses:

AD_1	AD_0	PORT SELECTED	FUNCTION
0	0	A	Read or Write PA
0	1	B	Read or Write PB
1	0	A	Write PA Data Direction
1	1	B	Write PB Data Direction

Since the data direction registers for PA and PB are each 8-bits, any pin on PA or PB may be programmed as input or output (0 = in, 1 = out).

Note: ① During ALE time the data/address lines are duplicated on A_{15}-A_8.

AC CHARACTERISTICS

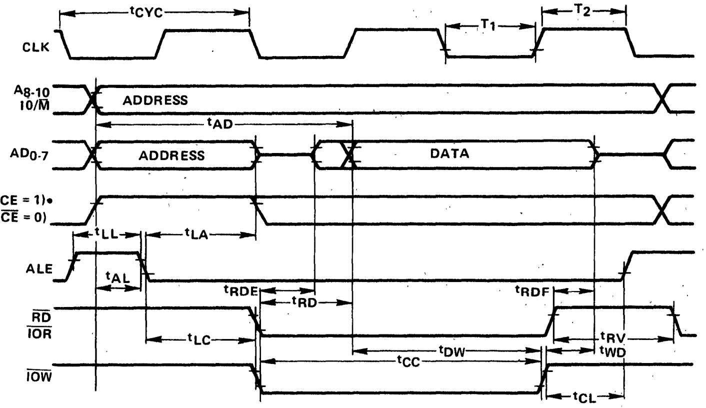
$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Cycle Time	t_{CYC}	320			ns	C_{LOAD} = 150 pF
CLK Pulse Width	T_1	80			ns	
CLK Pulse Width	T_2	120			ns	
CLK Rise and Fall Time	t_f, t_r			30	ns	
Address to Latch Set Up Time	t_{AL}	50			ns	150 pF Load
Address Hold Time After Latch	t_{LA}	80			ns	
Latch to READ/WRITE Control	t_{LC}	100			ns	
Valid Data Out Delay from READ Control	t_{RD}			170 ① 150 ②	ns	
Address Stable to Data Out Valid	t_{AD}			400	ns	
Latch Enable Width	t_{LL}	100			ns	
Data Bus Float After READ	t_{RDF}	0		100	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20			ns	
READ/WRITE Control Width	t_{CC}	250			ns	
Data In to WRITE Set Up Time	t_{DW}	150			ns	
Data In Hold Time After WRITE	t_{WD}	10			ns	
WRITE to Port Output	t_{WP}			400	ns	
Port Input Set Up Time	t_{PR}	50			ns	
Port Input Hold Time	t_{RP}	50			ns	
READY HOLD TIME	t_{RYH}	0		160 ① 120 ②	ns	
ADDRESS (CE) to READY	t_{ARY}			160	ns	
Recovery Time Between Controls	t_{RV}	300			ns	
Data Out Delay from READ Control	t_{RDE}	10			ns	

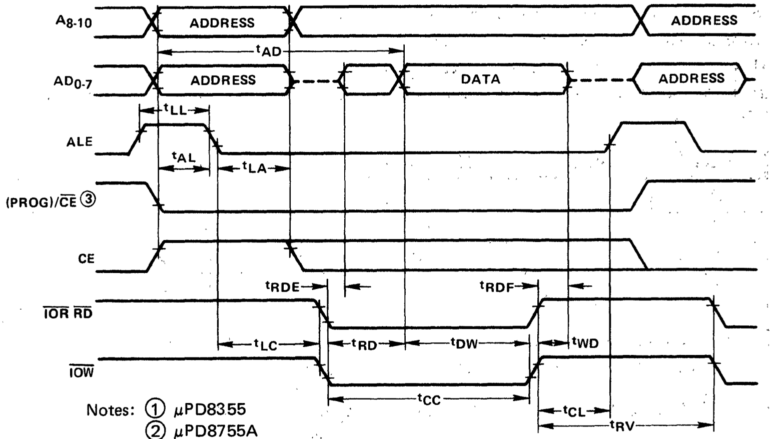
Notes: ① μPD8355
② μPD8755A

TIMING WAVEFORMS

ROM READ, I/O READ AND WRITE ①



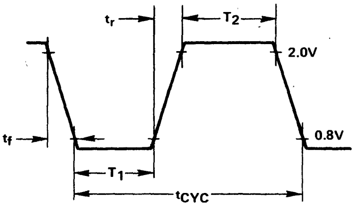
PROM READ, I/O READ AND WRITE ②



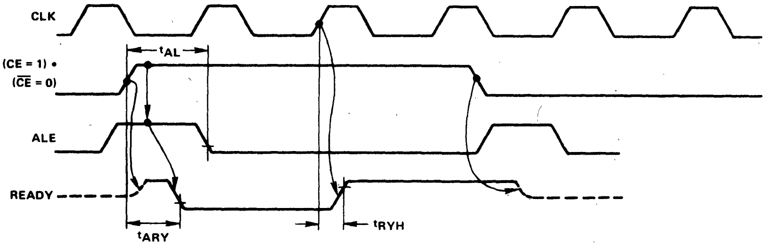
Notes: ① μPD8355
② μPD8755A
③ CE must remain low for the entire cycle

TIMING WAVEFORMS (CONT.)

CLOCK

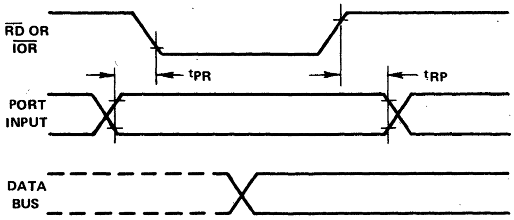


WAIT STATE TIMING (READY = 0)

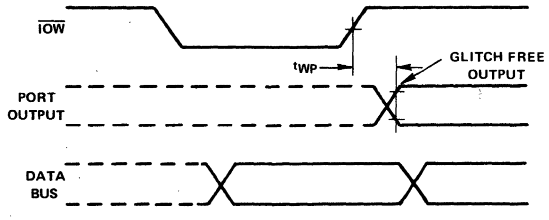


I/O PORT

INPUT MODE:



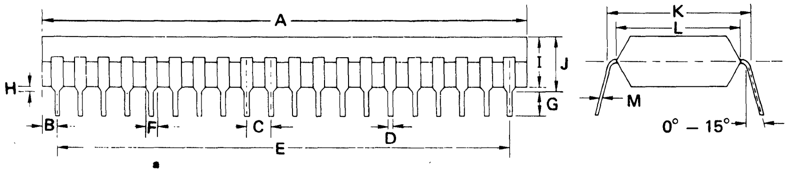
OUTPUT MODE:



EPROM PROGRAMMING μPD8755A

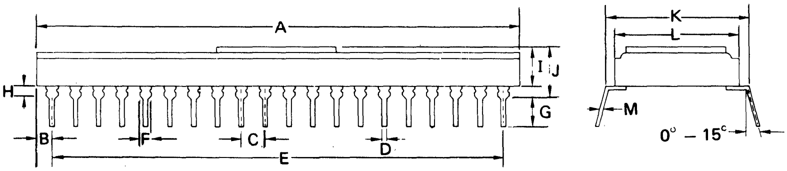
Erasure of the μPD8755A occurs when exposed to ultraviolet light sources of wavelengths less than 4000 Å. It is recommended, if the device is exposed to room fluorescent lighting or direct sunlight, that opaque labels be placed over the window to prevent exposure. To erase, expose the device to ultraviolet light at 2537 Å at a minimum of 15 W-sec/cm^2 (intensity X expose time). After erasure, all bits are in the logic 1 state. Logic 0's must be selectively programmed into the desired locations. It is recommended that NEC's prom programmer be used for this application.

PACKAGE OUTLINE
μPD8355C
μPD8755AD



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



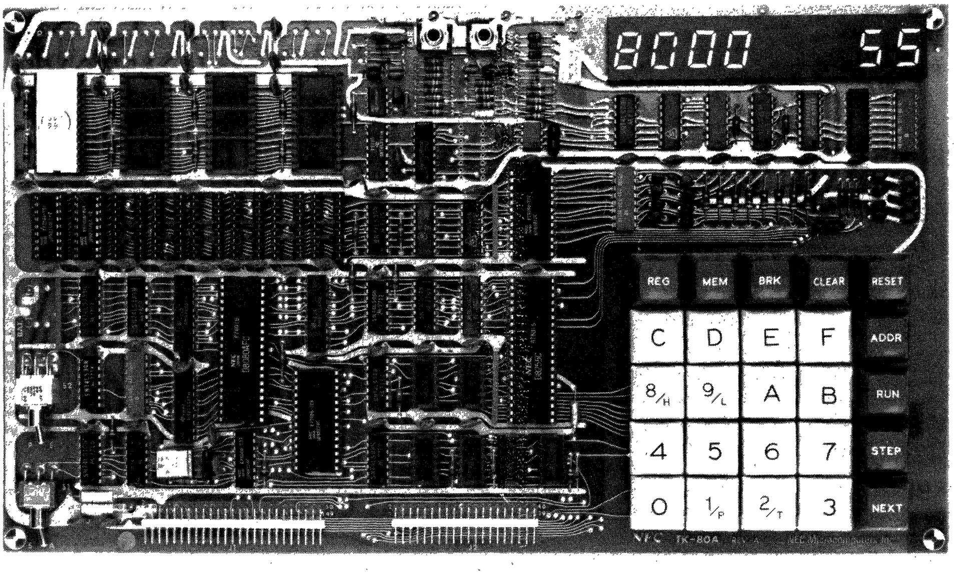
Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

TK-80A

DESCRIPTION The TK-80A is a single-board computer based on NEC Microcomputers' industry standard μPD8080AF. It facilitates understanding and developing 8080A systems and assembly language programs, and consists of the following blocks:

- μPD8080A Microprocessor Chip Set
- Monitor and User ROM
- RAM
- DMA Display
- Programmable I/O
- 25 Key Keyboard
- Tape Cassette Interface



TK-80A

µPD8080A MICROPROCESSOR CHIP SET

The µPD8080AF Processor, µPB8224 Clock Generator and Driver and the µPB8228 System Controller and Bus Driver comprise the 8080A chip set. The 8080A executes programs stored in memory and supports a large instruction set detailed in the µCOM-8 Software Manual. The 8224, coupled with an 18.000 MHz crystal, provides the 2.0 MHz, non-overlapping two-phase MOS clocks required by the 8080A. The 8224 also provides latches for synchronizing the RESET IN and READY IN signals. The 8228 provides bi-directional data bus drivers which buffer the 8080A data bus for on-board and external use. The 8228 also provides a Status Latch and gating array which provide active low memory and I/O read/write strobes, an Interrupt Acknowledge Strobe, and a data control bus enable input. The 8080A address bus is buffered by 3-state low power Schottky drivers with their enable pins tied to the bus enable input of the 8228, thus allowing the address, data and control busses to be asynchronously disabled by a single control line for user DMA.

MONITOR AND USER ROM/PROM

The TK-80A resident monitor is provided in NEC Microcomputers' 1K x 8 electrically erasable read-only memory, the µPD458. Since the 2708 and 458 are pin compatible when installed, (pin 1 to pin 1), either 2708's or 458's may be used to expand the ROM/PROM space. Through proper manipulation of on-board jumpers, any of the following devices may be used:

P/N	ORGANIZATION	TYPE	SUPPLIES ①
458	1K x 8	EEPROM	+12, +5
2708	1K x 8	EPROM	+12, +5, -5
2308	1K x 8	Mask ROM	+12, +5, -5
2758	1K x 8	EPROM	+5
2716	2K x 8	EPROM	+5
2316E	2K x 8	Mask ROM	+5
2732 ②	4K x 8	EPROM	+5
2332 ②	4K x 8	Mask ROM	+5

Notes: ① Read Mode.

② 0000 through 0FFF only. (All addresses in hexadecimal notation.)

RAM

The standard configuration TK-80A has 1K bytes of socketed RAM (2 pieces µPD2114LC) located at 8000 through 83FF. Up to 3K additional RAM may be installed in the sockets dedicated to locations 8400 through 8FFF. All memory and port address decoding is completely implemented to ensure that all possible expansion options are available to the user. The Protect/Enable switch provides for the connection of battery backup to all on-board RAM. If data must be retained for long periods of time with power off, the use of the NEC's 2114-compatible µPD444 CMOS RAM is recommended.

DMA DISPLAY

In order to improve throughput and demonstrate Direct Memory Access through "Hidden Refresh", the TK-80A uses an 8-byte block of RAM to control the 8-digit LED display directly. Data bytes, whose bits correspond one-for-one to display segments, are stored in display RAM, where they are directly accessed for display.

PROGRAMMABLE I/O

The µPD8255 Programmable Peripheral Interface provides the TK-80A with 24 I/O lines. Because the 8255 is a very flexible I/O device, the TK-80A can support considerable user I/O in addition to the Keyboard, Cassette and Display. The 8255 is located at Port Addresses 0F8 through 0FB, thus leaving both conventional and bit select decoding methods open for user expansion.

TAPE CASSETTE INTERFACE

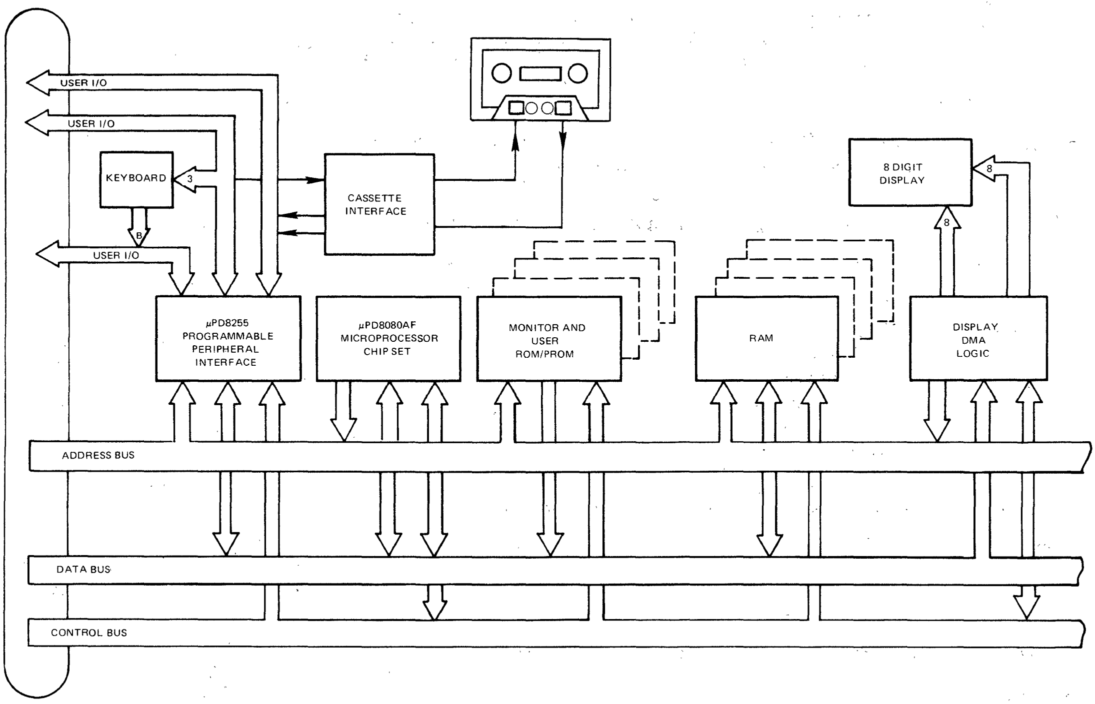
The on-board "Kansas City" compatible interface provides means for reliable, inexpensive mass storage using an audio cassette tape recorder. The data transfer rate is software selectable at 300 or 1200 baud. Jumpers in the interface circuitry allow the user to modify record and play back signal polarities to accommodate most tape recorders.

EXPANSION CONNECTORS

A 50 pin header, J1, for use with flat cable, allows expansion of the TK-80A for use with the EB-80A Expansion Board or other user circuitry. Buffered Address, Data and Control lines, as well as most commonly used interface signals, are available on J1.

J2, a 40 pin header, provides access to the on-board 8255. The 8255 input/output lines can be buffered and/or terminated with optional circuitry installed in sockets provided. Additional interface signals and a 2400 or 1200 Hz interrupt clock are also available on J2.

BLOCK DIAGRAM



HARDWARE SPECIFICATIONS

- Word Size
  - Instruction: 1, 2, or 3 8-Bit Bytes
  - Data: 8 Bits
- System Clock: 2 MHz ± 0.1%
- Cycle Time
  - Basic Instruction Cycle: 2.0 μs ①
  - Maximum Instruction Cycle: 9.0 μs
- Processor Chip Set
  - Processor: μPD8080AF
  - Clock: μPB8224
  - Bus Control: μPB8228

Note: ① Basic Instruction Cycle is defined to be the shortest instruction, i.e., four clock cycles.

MEMORY ADDRESSES

On-Board ROM/PROM	0000 – 03FF (Monitor)
On-Board RAM	8000 – 83FF

MEMORY CAPACITY

On-Board ROM/PROM:	4K Bytes using 1K Memories 8K Bytes using 2K Memories
On-Board RAM:	4K Bytes in 1K Increments
Off-Board Expansion:	Up to 64K Bytes Total

I/O ADDRESSES

On-Board Programmable I/O Controller: μPD8255

Port	A	B	C	Control
Address	F8	F9	FA	FB

I/O CAPACITY

- Parallel: 24 Lines
  - Expansion to a total of 48 I/O lines (34 uncommitted) is possible using the optional EB-80A Expansion Board and to 256 Ports using customer supplied circuitry.
- Compatible with: 7400, 7403, 7408, 7409, 7426, 7432, 7437 and 7438.
- Cassette:
  - "Kansas City" Compatible
  - 8-Bit Characters
  - One Start Bit and Two Stop Bits
  - 300 or 1200 Baud (Software Select)
  - Sinusoidal FSK Recording
  - Logic "0" – 1200 Hz
  - Logic "1" – 2400 Hz
  - Output 30 mV or 3V Peak-to-Peak
  - Input – 0.3 – 10V Peak-to-Peak, 2V Peak-to-Peak Nominal

DISPLAY

• Number:	8 Digits
• Size:	0.5 in (1.27 cm)
• Type:	LED Seven Segment with Right-Hand Decimal

KEYBOARD

- Keyswitches: Gold Contact Crossbar Type, 0.150 in travel
- Keytops: Double-Shot Removable

INTERRUPTS

On-board logic may be used to auto-vector the processor to 0038 using RESTART 7. External user logic may be used to supply 3-byte interrupts that vector to any memory location.

INTERFACES

- Fully TTL Compatible
- Address and Data Bus
- Control Bus
- Parallel I/O
- Interrupt Request
- Interrupt Clock Available: 2400 Hz – TTL Compatible

HARDWARE SPECIFICATIONS (CONT.)

CONNECTORS

- Power: 1 piece 4 conductor nylon crimp type, 0.156 centers Molex 09-50-7041 or equivalent (supplied)

  4 pieces terminals, crimp, loose Molex 08-50-0106 or equivalent (supplied)
- Bus: 50 conductor flat cable connector
  3M 3425-0000 or equivalent
- Parallel I/O: 40 conductor flat cable connector
  3M 3417-0000 or equivalent
- Cassette: In and Out: Standard 1/8" miniature phone plug
  Switchcraft "Tini-Plug" 750 or equivalent

PHYSICAL CHARACTERISTICS

- Width: 13.00 in (33.02 cm)
- Depth: 1.40 in (3.56 cm)
- Height: 7.50 in (19.05 cm)
- Weight: 18 oz (510.3 gm)

ELECTRICAL CHARACTERISTICS

DC POWER ①	WITHOUT DISPLAY	WITH DISPLAY ②
$V_{CC} = +5V \pm 5\%$	1.1 A max	1.5 A max
$V_{DD} = +12V \pm 5\%$	150 mA max	150 mA max
$V_{BB} = -5V \pm 5\%$	③④	③④

Notes: ① Standard configuration with 1K EEPROM and 1K RAM.

② All segments and decimal points of all digits on.

③ For ROM/PROM, RAM and I/O Expansion power consumption, refer to specific data sheets.

④ V_{BB} for the μPD8080AF and one 2708 is generated from V_{DD} and regulated onboard. V_{BB} may be externally supplied via 4-conductor power connector.

ENVIRONMENTAL

- Operating Temperature: 0°C to +50°C

TK-80A

COMMAND FUNCTIONS

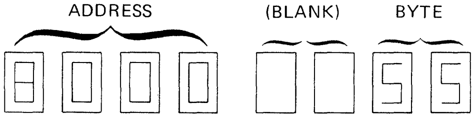
- Display and/or Modify Memory
- Display and/or Modify Registers
- Run User-Written Programs
- Read and Write Cassette Tapes of Memory Images

KEY IDENTIFICATION

KEY	USAGE
ADDR	In most commands, before entering an address value
CLEAR	At any time, to change an entry
NEXT	After some commands, to advance an address pointer
MEM	After an address value, before entering a new memory value
STEP	After an address value, or a previous STEP, to single-step one instruction in a user program
RUN	After an address value, to run a user program in breakpoint or free-running mode
BRK	After an address value which becomes the breakpoint, before entering the breakpoint depth value
REG	Before entering a register name
RESET	To reset all hardware and execute at 0000
0-9, A-F	Hexadecimal value keys

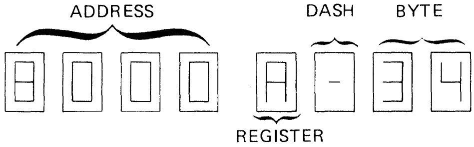
DISPLAY MODES

MEMORY MODE



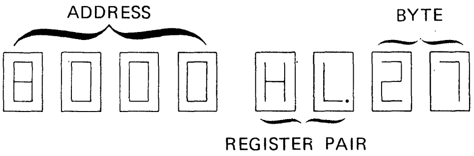
- the ADDRESS field displays a selected memory location address.
- the BYTE field displays the contents of memory at that address.

REGISTER MODE



- the ADDRESS field displays the contents of the user-program program counter.
- the REGISTER field displays the name of a selected processor register; A, B, C, D, E, F, H, L.
- the BYTE field displays the contents of that register.

REGISTER-PAIR MODE



- the REGISTER-PAIR field displays the name of a selected register-pair; BC, DE, HL, SP (stack pointer) or ST (top of stack).
- the ADDRESS field displays the contents of the selected register-pair.
- the BYTE field displays the contents of the memory location whose address is displayed in the ADDRESS field.

CASSETTE TAPE MASS STORAGE/MEMORY BACKUP

- 1200 Baud is Default Rate
- 300 Baud is Software Selected for Full Kansas-City Standard
- Tape Contains a Block of Consecutive Memory Images, Followed by a Checksum Byte.
- Checksum is Generated Automatically During Record; Checksum is Verified During Playback.

MEMORY MAP

ADDRESS	MEMORY SIZE	USAGE
0000-03FF	1K	ROM Monitor
0400-0FFF	3K	On-Board ROM Sockets for User Expansion
1000-1FFF	4K	Optional ROM Area ①
2000-7FFF	24K	Unused Area
8000-839F	928	User's RAM Area
83A0-83F7	88	Monitor's RAM Work Area
83F8-83FF	8	LED Display
8400-8FFF	3K	On-Board RAM Sockets for User Expansion
9000-FFFF	28K	Unused Area

Note: ① On-board ROM sockets may be jumpered for up to 8K total.

PROCEDURE FOR ENTERING AND DEBUGGING PROGRAM

1. A program is first written by the user to perform a desired function. This program is assembled manually into 8080A instructions and entered into consecutive locations in RAM via the keyboard.
2. Next the program is run, under monitor control, in single-step mode with the Step/Auto switch in the Step position. Only one user program instruction is executed at a time. After each instruction, the display informs the user of the results.
3. During the debugging process, expected results can be checked by displaying memory or registers. Registers are saved upon entry to the monitor and restored upon exit to the user program. The register values may be altered or displayed.
4. When only a few bugs remain in the user program, the program may be run in breakpoint mode. Alternatively, the user program may be executed in a free-running mode, without monitor control. In the free-running mode, however, the Step/Auto switch should be in the Auto position. This mode permits instruction execution at the full speed of the μPD8080AF.
5. The program can be saved on a tape for future use by using the monitor WRITE program. Memory is saved as a block of consecutive locations followed by a monitor-generated checksum, which is displayed at the completion of the write sequence.

   To restore the contents of memory, the monitor READ program is used. The checksum which is read from the tape is compared with the checksum calculated during playback, and the two values are displayed. If a visual comparison indicates both checksums are the same, the correct data transfer may be assumed.

TK-80A

MEMORY RESOURCE USAGE

Memory Requirements:

- μPD458 ROM – monitor resides in 1K at 0000 – 03FF.
- μPD2114L RAM – RAM work area, including stack, at 83A0 – 83F7.
- Display output generated by hardware DMA at 83F8 – 83FF.
- μPD8255 Input/Output

PORT ADDRESS	USAGE
F8	Port A: keypad row input
F9	Port B: Bit 0: Cassette serial input Bit 7: Cassette zero-crossing feedback
FA	Port C: Bit 0: Cassette serial output Bit 4, 5, 6: keypad column strobe output
FB	I/O mode control; Port C bit set/reset control

MONITOR SUBROUTINES

NAME	JUMP VECTOR ADDRESS	FUNCTION	PARAMETERS
DISPLAY			
CL	03CF	clear LED display digits	number of LED digits in B
MSG	03D2	display an 8-digit message	address of message in HL
DLADE	03E1	display a byte as two hexadecimal digits	byte value in A; digit position in DE
DLHLDE	03E4	display a word as four hexadecimal digits	word value in HL; digit position in DE
DLHEX	03E7	display a nibble (half-byte) as one hexadecimal digit	nibble value in bits 0-3 of A; digit position in DE
KEYBOARD			
GETW	03EA	get a 4-digit hexadecimal word	word value in HL; key count in D; terminator key in A and B
GETB	03ED	get a 2-digit hexadecimal byte	byte value in L; key count in D; terminator key in A and B
KEY	03F3	get any debounced key	key value in A and C; carry set if hexadecimal key
KYBD	03F0	get an immediate key closure	carry set if key found; key value in A
CASSETTE INTERFACE			
SERIN	03D5	read a byte from cassette	byte value in D; carry set if error
SEROT	03D8	write a byte to cassette	byte value in C
RTP	03DB	read formatted block into memory	start address in HL; end address in DE; carry set if error
WTP	03DE	write formatted block from memory	start address in HL; end address in DE
OTHER			
D1MS	03F6	delay one millisecond	none
READ	03F9	stand-alone read tape program	start address in HL; end address in DE
WRITE	03FC	stand-alone write tape program	start address in HL; end address in DE

ROM ORDERING PROCEDURE — MEMORIES AND MICROCOMPUTERS

The following NEC products fall under the guidelines set by the ROM Ordering Procedure:

µPD2316E
µPD2332
µPD2364
µPD8021
µPD8041
µPD8048
µPD8049
µPD8355
µPD546
µPD547
µPD547L
µPD548
µPD550
µPD551
µPD554
µPD650
µPD651
µPD652

In order to facilitate the transferal of ROM mask information, NEC Microcomputers, Inc., is able to accept mask patterns in a variety of formats. These are intended to suit various customer needs and minimize the turnaround time. The following is a list of valid media for code transferal.

- Sample ROMs or ROM-based microcomputers
- PROM/EPROM equivalent to ROM parts
- NEC µPD458 EEPROM
- BNPF Paper Tapes
- Hex Paper Tapes
- Timesharing Files
- Other (Contact NEC Microcomputers, Inc., for arrangements.)

Thoroughly tested verification procedures protect against unnecessary delays or costly mistakes. NEC Microcomputers, Inc., will return the ROM mask patterns to the customer in the most convenient format. Unprogrammed EPROMs, where applicable, if sent with the ROM code can be programmed and returned for verification. HEX paper tapes with the listing are the most convenient means of verification.

Earth satellites and the world-wide GE Mark III timesharing systems provide reliable and instant communication of ROM patterns to the factory. Customers with access to GE-TSS may further reduce the turnaround time by transferring files directly to NEC Microcomputers, Inc.

The following is an example of a ROM mask transferal procedure. The µPD8048 is used here, however the process is the same for the other ROM-based products.

1. The customer contacts NEC Microcomputers, Inc., concerning a ROM pattern for the µPD8048 that he would like to send.

2. Since an EPROM version of that part is available, the 8748 is proposed as a code transferal medium, or alternatively, a paper tape and listing.

3. The paper tape and a blank 8748 for verification are sent to NEC Microcomputers, Inc.

4. NEC Microcomputers, Inc., reads the tape, programs the 8748, and enters the code into GE-TSS, returning the 8748 to the customer.

5. Once the customer notifies NEC Microcomputers, Inc., in writing that the code is verified, work commences immediately on the development of his µPD8048s.

NEC Microcomputers, Inc.

NEC

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NEC

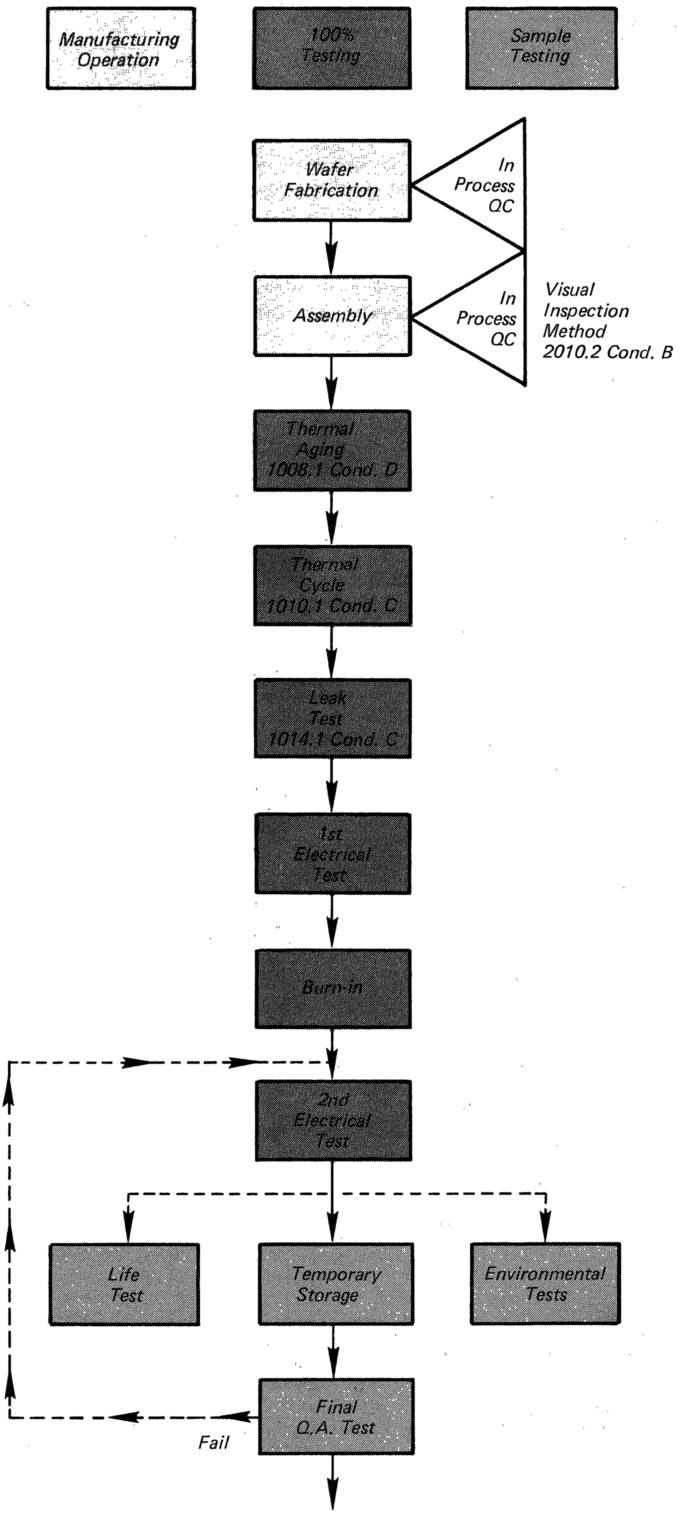
NEC Quality Assurance Procedures

One of the important factors contributing to the final quality of our memory and microcomputer components is the attention given to the parts during the manufacturing process. All Production Operations in NEC follow the procedures of MIL Standard 883A. Of particular importance to the reliability program are three areas that demonstrate NEC's commitment to the production of components of the highest quality.

I. Burn-In — All memory and microcomputer products are dynamically burned in at an ambient temperature sufficient to bring the junction to a temperature of 150 °C. The duration of the burn-in is periodically adjusted to reflect the production history and experience of NEC with each product. 100% of all NEC memory and microcomputer products receive an operational burn-in stress.

II. Electrical Test — Memory and microcomputer testing at NEC is not considered a statistical game where the device is subjected to a series of pseudo random address and data patterns. Not only is this unnecessarily time consuming, but it does not effectively eliminate weak or defective parts. NEC's test procedures are based on the internal physical and electrical organization of each device and are designed to provide the maximum electrical margin for solid board operation. For further information on NEC's testing procedures see your local NEC representative.

III. After completion of all 100% test operations, production lots are held in storage until completion of two groups of extended sample testing: an operating life test and a series of environmental tests. Upon successful completion of these tests, the parts are released from storage and sent to final Q.A. testing.



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